

# Accelerated Quantum Monte Carlo with Probabilistic Computers

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Quantum Monte Carlo (QMC) techniques are widely used in a variety of scientific problems of great interest and much work has been dedicated to developing optimized algorithms that can accelerate QMC on standard processors (CPU). In this paper, we demonstrate 2 – 3 orders of magnitude acceleration of a standard QMC algorithm using a specially designed digital processor, and a further 2 – 3 orders of magnitude by mapping it to a clockless analog processor. Similar improvements through customized hardware design have been demonstrated for other applications. Our demonstration provides a roadmap for 5-6 orders of magnitude acceleration for a transverse field Ising model (TFIM) and could possibly be extended to other QMC models as well. The clockless analog hardware can be viewed as the classical counterpart of the quantum annealer and provides performance within a factor of  $< 10$  of the latter. The time to solution (TTS) for the clockless analog hardware scales with the number of qubits as  $O(N)$ , improving the  $O(N^2)$  scaling for CPU implementations, but appears worse than that reported for quantum annealers by D-Wave.

## I. INTRODUCTION

Envisioned by Feynman [1] and later formalized by Deutsch [2] and others [3], quantum computing has been perceived by many as *the natural simulator* of quantum mechanical processes that govern natural phenomena. It became more popular with the discovery of powerful algorithms like *Shor's integer factorization* [4] and *Grover's search* [5] offering significant theoretical speedup over their classical counterpart. A different flavor of quantum computing was also theorized in [6–9] which makes use of the *adiabatic theorem* [10]. It was later shown that these two flavors of quantum computing are equivalent [11]. The technological difficulties of realizing noiseless qubits with coherent interactions among the qubits have focused recent efforts on the Noisy Intermediate Scale Quantum (NISQ) regime [12] and serious progress has been made in recent years [13–19].

In the absence of general-purpose quantum computers, quantum Monte Carlo (QMC) still remains the standard tool to understand quantum many-body systems and to investigate a wide range of quantum phenomena – including magnetic phase transitions, molecular dynamics, and astrophysics [20–23]. Much effort has been made to develop efficient QMC algorithms of various sorts [22–31] which can be suitably implemented on standard general-purpose classical processors (CPU). Interestingly for many important quantum problems, the efficiency of QMC is significantly affected by the notorious *sign problem* [32]. The sign problem manifests itself as an exponential increase in the number of Monte Carlo (MC) samples required to reach convergence [33]. The origin of the problem is that qubit wavefunctions can destructively interfere in the Hilbert space. Quantum problems that do not pose a sign problem are given a special name *stoquastic* and it is believed *non-stoquasticity* is an essential ingredient for AQC to be universal [11] and to provide significant speedup over classical computers [34, 35].

Recently in [36], King et al. demonstrated that with a physical quantum annealing (QA) processor, it is possible to achieve 3 million times speed up with scaling advantage over an optimized cluster-based continuous time (CT) path integral Monte Carlo (PIMC) code simulated on CPU. In a stunning demonstration, King et al. applied the Transverse Field Ising (TFI) Hamiltonian on a geometrically frustrated lattice initialized with a *topologically obstructed* state. This obstruction makes it difficult for an algorithm based on local update schemes to escape the obstruction, whereas a quantum annealer might help escape the obstruction faster. This is interesting because until this result, results on TFI, a well-known stoquastic Hamiltonian, have been routinely benchmarked with quantum Monte Carlo algorithms [37] with no clear scaling differences for practical problems [38]. In the theoretical CS community, the possibility of obtaining a scaling advantage for AQC with sign- problem-free Hamiltonians (such as TFI) is still being actively discussed [39, 40].

PIMC, one of many variations of QMC, is the state-of-the-art tool for simulating and estimating the equilibrium properties of these quantum problems. Powerful and efficient cluster-based algorithms exist for ferromagnetic spin lattices [41]. However, it is known that the efficiency of the cluster algorithms drops when frustrations are introduced in the lattice although alternative approaches that compromise between local and global updates were explored [42] in the context of the classical Ising model.

## Outline of paper

In this paper, we explore the possibility of hardware accelerating QMC with a processor based on probabilistic bits (p-bits) which can be viewed as a classical counterpart of the QA processor [43]. A p-bit is a robust, classical, and room-temperature entity that continuously fluctuates between two logic states and the rate of this

fluctuation can be controlled via an input signal applied to a third terminal [44]. p-bits can also be made very compact and can provide true randomness (important for the problem we address in this paper, see Appendix E) instead of pseudo-random generators, commonly used in software-based solutions.

We start in Section II with a description of the benchmarking example used in [36] to show the scaling advantage compared to CPU. We then describe the design of an optimized probabilistic computer using the discrete-time (DT) PIMC method in accordance with Suzuki-Trotter approximation with enough replicas to provide adequate accuracy (Section III). This design makes use of massive parallelism and appropriate synapse to maximize the number of samples collected per clock cycle resulting in 3 orders of magnitude improvement in TTS on a state-of-the-art FPGA over TTS on a CPU. Next in Section IV, we translate the digital circuit into a clockless mixed-signal design with fast resistive synapses and low barrier magnet (LBM) based compact p-bit and use SPICE simulations based on experimentally benchmarked models to project another 2 to 3 orders of magnitude speedup. Figure 1 illustrates these four different hardware and their relative expected performances.

Our demonstration provides a roadmap for 5 to 6 orders of magnitude acceleration for a transverse field Ising model (TFIM) and could possibly be extended to other QMC models as well. The clockless analog hardware can be viewed as the classical counterpart of the quantum annealer and provides performance within a factor of  $< 10$  of the latter. The time to solution (TTS) for the clockless analog hardware scales with the number of qubits as  $\sim N$ , which is better than the  $\sim N^2$  scaling for CPU implementations, but appears worse than that reported for quantum annealers (Section V), thus providing independent evidence for the possibility of improved scaling of quantum processors over classical ones even for stoquastic problems.

## II. DESCRIPTION OF THE QUANTUM PROBLEM

We emulate a quantum problem from a recent work ([36]) where a Transverse Field Ising (TFI) Hamiltonian (which is stoquastic)

$$\mathcal{H}_{\mathcal{Q}} = - \left( \sum_{\langle ij \rangle} J_{ij} \sigma_i^z \sigma_j^z + \Gamma \sum_i \sigma_i^x \right) \quad (1)$$

is applied over a two-dimensional square-octagonal qubit lattice as shown in Fig. 2(a). The exotic physics offered by this qubit lattice is of practical interest and has been described in [36, 45]. The square-octagonal lattice can be viewed as a  $(2L - 6) \times L$  antiferromagnetically (AFM) coupled triangular lattice with a four ferromagnetically (FM) coupled spin basis, giving rise to a total of  $4L(2L - 6)$  qubits in the lattice. The resulting lattice consists of

square and octagonal plaquettes which are periodically connected along one direction and has open boundaries in the other direction. In the bulk of the lattice, each qubit is connected to three other neighbors whereas at the open boundary, some qubits are connected to just one neighbor and the others are connected to two neighbors. To increase degeneracy in the Hilbert lattice, the AFM couplings at the open boundary are also reduced to half of that in the bulk.

Each square or octagonal plaquette in this lattice is composed of qubits from three different sublattices and has an odd number (three for octagonal plaquettes and one for square plaquettes) of AFM bonds. This leads to a frustrated lattice since it is impossible to satisfy all the bonds simultaneously. Three different qubit sublattices within the lattice are indicated by the red, green, and blue colors in Fig. 2(a).

### Defining the observable

In this benchmark study, we observe the *average equilibration speed* of *average order parameter* when initialized with a particular classical state (in this study we will be referring to two particular initial states: CCW and ordered, see Appendix A for more details) in probabilistic computer. We will compare this result against general purpose processor (CPU) and with the quantum annealing processor from [36]. The procedure to obtain the average order parameter was defined in [36]. For the sake of completeness, we provide the details of it in the following:

1. Average of four FM-coupled qubits are computed for each basis in the lattice. Depending on the sublattice the basis belongs to, these averages are denoted as  $m_{\text{av,red}}$ ,  $m_{\text{av,green}}$  or  $m_{\text{av,blue}}$  (see Fig. 2). As mentioned earlier, averaging over basis turns the lattice into an AFM-coupled triangular lattice.
2. For each triangular plaquette in the transformed triangular lattice (including those formed from periodic boundary), compute the complex valued quantity known as *pseudospin* which is defined as follows:

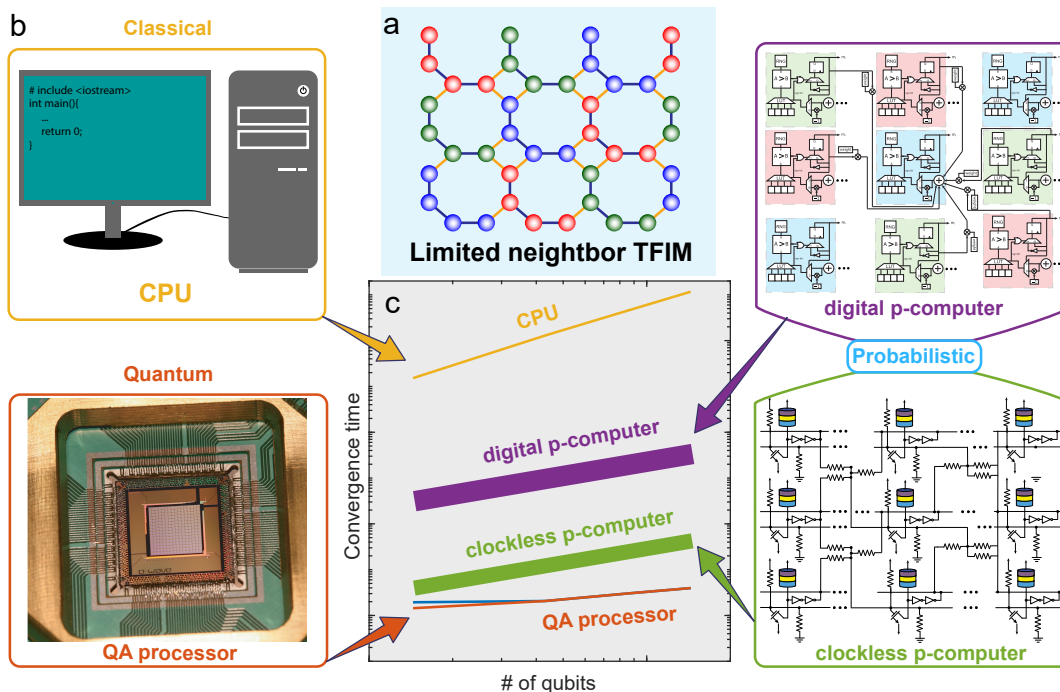
$$\zeta_{\text{pl}} = \frac{1}{\sqrt{3}} (m_{\text{av,red}} + e^{i2\pi/3} m_{\text{av,green}} + e^{i4\pi/3} m_{\text{av,blue}}), \quad (2)$$

3. Average over all triangular plaquettes, i.e.,

$$\zeta_{\text{conf}} = \sum_i \zeta_{\text{pl},i} \quad (3)$$

4. Obtain the average order parameter by taking the average of absolute values for different configurations of the lattice, i.e.,

$$\langle m \rangle = \sum_k p_k |\zeta_{\text{conf},k}| \quad (4)$$



**FIG. 1. Performance of specially designed p-computers, digital and clockless, relative to a CPU and a quantum annealer:** (a) We use an example problem consisting of a lattice of qubits described by a transverse field Ising model (TFIM). We simulate it classically using the Suzuki-Trotter transformation and calculate a pre-defined order parameter using three different types of hardware whose relative times to solution (TTS) are sketched in (c). The four types of hardware are shown schematically in (b): (1) a von Neumann machine (CPU) – which simulates the problem by breaking down the problem into a series of instructions and executing them sequentially one after another, (2) a physical quantum annealer (QA) that maps the problem onto a network of rf-SQUIDs emulating qubits and rf-couplers coupling those qubits (3) a digital p-computer built using FPGA to lay out a spatial network of interconnected probabilistic p-bits and (4) a clockless p-computer constructed by interconnecting a network of p-bits through resistors.

where  $p_k$  is the probability of occurrence for configuration  $k$ .

### III. DESIGNING THE PROBABILISTIC EMULATOR

Our p-computer is a discrete time path integral Monte Carlo (DT-PIMC) emulator based on the Suzuki-Trotter approximation [46]. The idea of such a hardware emulator for QMC was first proposed in [43]. In this scheme, one tries to approximate the partition function of the quantum Hamiltonian,  $Z_Q$ :

$$Z_Q = \text{tr} [\exp(-\beta H_Q)] \quad (5)$$

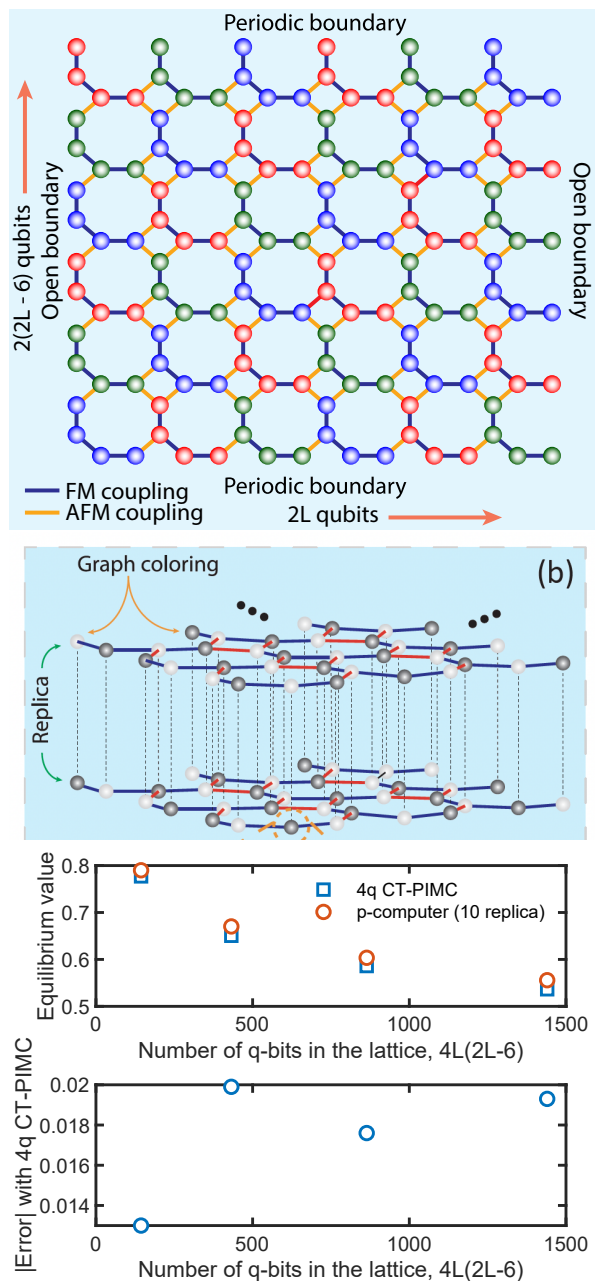
with a classical Hamiltonian,  $H_{Cl}$  such that the partition function of  $H_{Cl}$  is equal to  $Z_Q$ . For the Hamiltonian in Eq. (1), one finds that the following classical Hamiltonian,  $H_{Cl}$ :

$$H_{Cl} = - \sum_{k=1}^r \left[ \sum_{i < j} J_{\parallel, ij} m_{i,k} m_{j,k} + \sum_i J_{\perp} m_{i,k} m_{i,k+1} \right] \quad (6)$$

with  $J_{\parallel, ij} = J_{ij}/r$ ,  $J_{\perp} = -(0.5/\beta) \ln [\tanh(\beta\Gamma/r)]$  and  $m_{i,j} \in \{-1, +1\}$  yields the same  $Z_Q$  in the limit  $r \rightarrow \infty$ . The error going down as  $\mathcal{O}(1/r^2)$ , in practice, one can find a reasonably good approximation with a finite number of replicas in many cases.

We start the process of designing our p-computer with the trotterization of the qubit lattice using 10 replicas and involving  $40L(2L - 6)$  p-bits, ranging up to 14,400 p-bits for  $L = 15$ . Traditional Gibbs sampling or single flip Monte Carlo sampling takes too long to converge for such a big network and we need a scheme that allows us to simultaneously update many p-bits. But it is also well-known that updating two p-bits simultaneously which are connected to each other, leads to erroneous output. We realized that the limited connections among the p-bits in the replicated network can be utilized to achieve massive parallelism where many p-bits can be updated in parallel and therefore can be used to speedup the convergence. To obtain such massive parallelism, we next applied graph coloring on the replicated p-bit network, as recently explored in Ref. [47] for general and irregular lattices.

Graph coloring assigns different colors to p-bits that are connected to each other and ensures that no two p-bits that are connected to each other have the same



**FIG. 2. Example problem addressed in this paper following King et al. [36]:** (a) quantum problem solved on QA involves a two-dimensional square octagonal lattice of qubits having  $2L$  qubits in one direction and  $2(2L-6)$  qubits in the other direction (illustration shows  $L = 6$ ). The blue bond between two qubits denotes FM coupling ( $J_{\text{FM}} = -1.8$ ) and yellow bond indicates AFM coupling ( $J_{\text{AFM}} = 1.0$ ). The AFM couplings at the open boundary have  $J_{\text{AFM}} = 0.5$  (b) Trotterized mapping solved on classical computers, (c) Trotter error with 10 replicas: (Top) Equilibrium values predicted from 10 replica PPU emulation and 4q CT-PIMC algorithm developed in [36]. (Bottom) Absolute difference in predicting equilibrium values between the two methods.

color thus enabling us to update all p-bits in the same color group simultaneously. Although not immediately

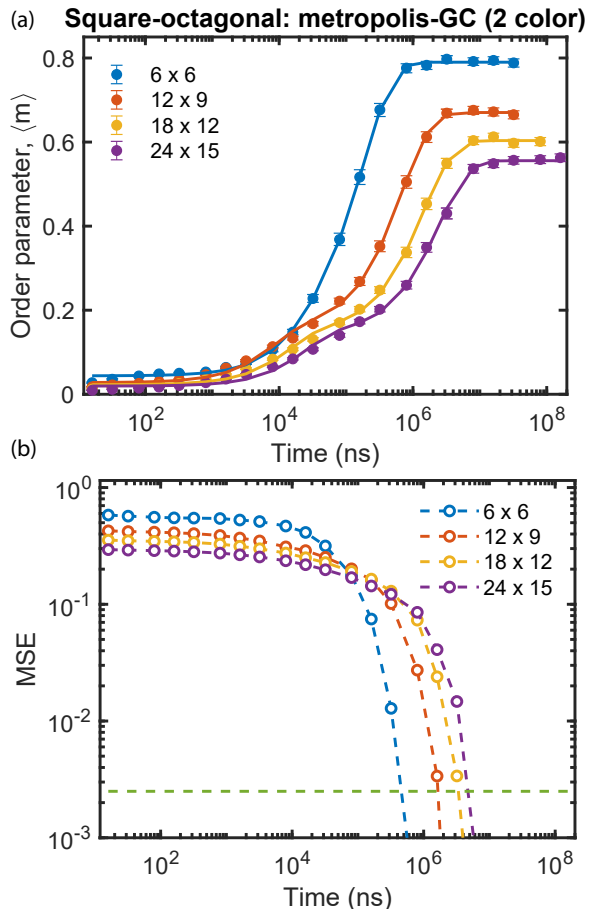
obvious, it can be easily checked that the qubits of the square-octagonal lattice under consideration can be colored using just two colors. If we always *choose even number of replica* (which is what we do in this work), then we found that the translated p-network can also be colored using just two colors as shown in Fig. 2(b). Hence with just two colors, half of the p-bit network can be updated in one clock cycle and the other half of the network in another, producing one sample in every two clock cycles. In general, compared to a single flip Monte Carlo implementation which updates one spin in one clock cycle, this graph-colored approach can reduce the number of clock periods required to converge by a factor of  $\sim nr/C$  ( $nr$  is the number of p-bits and  $C$  is the number of colors) assuming same clock period for both cases.

This leads us to argue that a p-computer should exhibit weaker dependence with the increasing size of the network compared to the CPU because even though the number of p-bit increases in the network, one can also proportionally increase the number of p-bits (we estimate that up to one million of p-bits can be integrated on a chip with a reasonable power budget [48]) to be updated in a given clock, yielding a factor of  $n$  ( $=$  number of p-bits in the network) improvement in scaling over CPU. This demonstrates the power of a properly architected p-computer over CPU where the scope of such parallelization is very limited.

### Digital p-computer emulation on FPGA

To demonstrate the utility of such massively parallel architecture, we next emulate this graph-colored p-bit network by implementing it on FPGA using Amazon Web Services (AWS) F1 instance (more details of the FPGA implementation can be found in the Appendix B). Various implementations of p-bits including digital and analog have been discussed in [48, 49]. The digital implementations of p-bits are costly in terms of resources and require thousands of transistors per p-bit and so we have only been able to fit the smallest lattice size ( $L = 6$ ) with the resources provided therein. But we expect that when replaced with nanomagnet-based s-MTJs, the situation would improve drastically. It is also equally important to carefully design the synapse that can provide updated information to p-bits by quickly responding to any changes in the state of neighboring p-bits. In the spirit of [50], we carefully choose our synapse to update  $nr f/C$  p-bits per second providing  $f/C$  samples per second. The clock period  $1/f$  needs to be minimized carefully so that the synapse can correctly calculate the response while providing maximum throughput. In our demonstrations, we have been able to run the smallest lattice with 8 ns clock period (16 ns per sample since we have two colors) and we believe that given enough resources we should also be able to run the bigger lattices at the same clock frequency. For the other lattice sizes, we obtain the average order parameter versus the number of samples plots

via running MATLAB on CPU (a verification of FPGA output matching MATLAB output is also provided in the Appendix B) and then multiply the  $x$  axis of that plot by 16 ns per sample. These lead to the curves in Fig. 3(a), where we report the average order parameter,  $\langle m(t) \rangle$  versus time curves obtained from p-computer emulation for the same four lattice sizes of square-octagonal lattice and with the same parameters as in [36] but only with CCW initial condition. The curves with CW initial condition are similar to these CCW curves (slightly faster than CCW) whereas curves for ordered initial condition (not shown) shows much faster convergence.



**FIG. 3. Extracting TTS from simulation results following the protocol described in [36]:** (a) Average order parameter  $\langle m \rangle$  as defined in Eq. (2) (Eq. (2) in [36]) are obtained for four different lattice sizes using the mapped p-bit network. We have used  $\Gamma = 0.736$ , and  $\beta = 1/0.244$  for which the scaling difference was reported to be maximum. We show results only for ‘CCW’ initial condition as explained in the Appendix A). All data points are averaged over 1000 different runs and the errorbars correspond to 95% confidence interval around the mean. The dashed lines represent  $a \exp(-bx) + c \exp(-dx) + g$  type fit. (b) Mean squared error (MSE) plot for each lattice sizes from their corresponding ‘ $g$ ’ values in (a). The scaling is more clearly visible in this plot. Also shown is the 0.0025 threshold in dashed green which is used to define convergence.

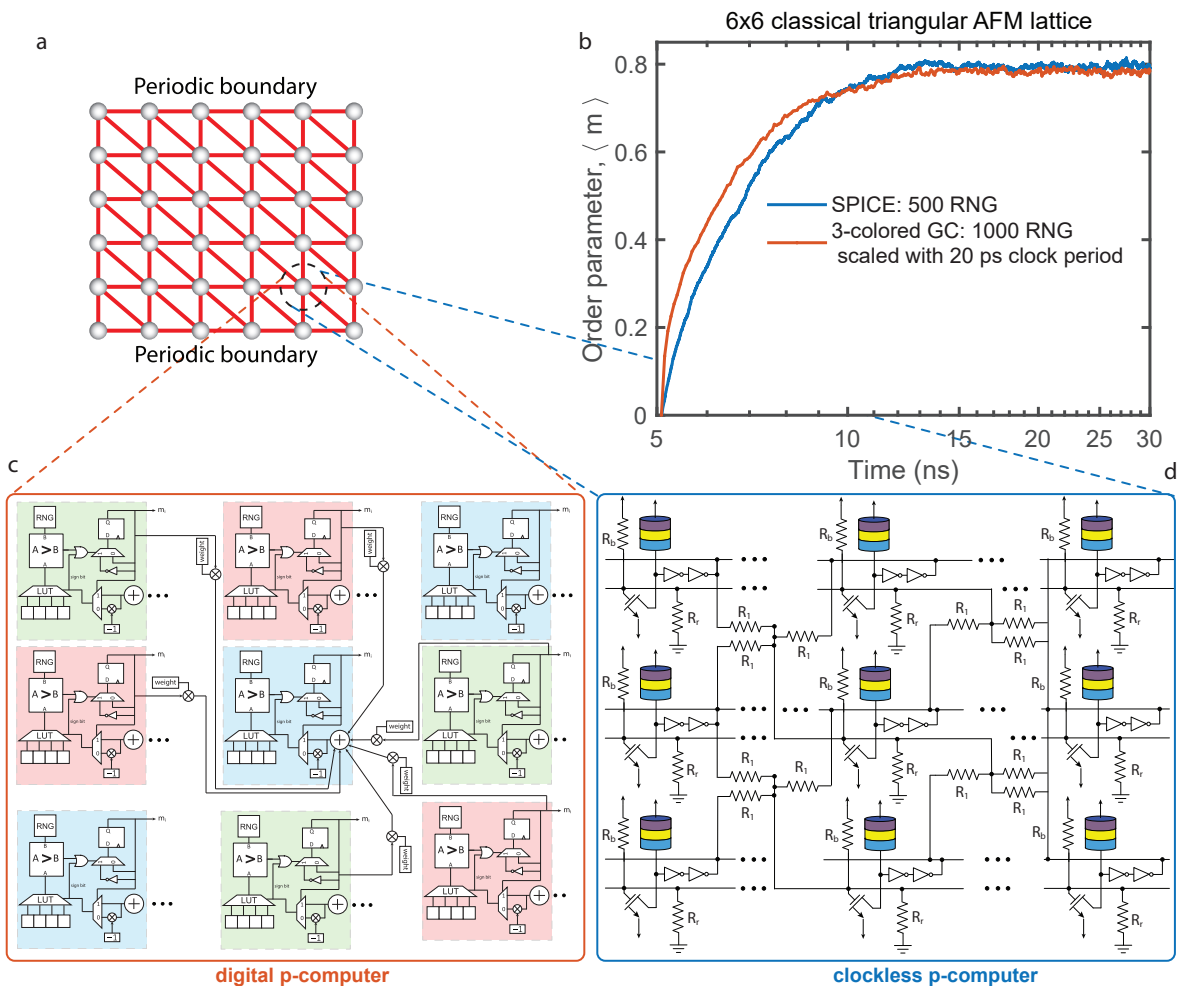
**Data fitting and convergence criterion:** Each curve in Fig. 3(a) is then fitted with  $ae^{-bx} + ce^{-dx} + g$  type fitting model (a justification for using this fitting model is provided in the Appendix C) where  $g$  represents the prediction for equilibrium value of average order parameter from p-computer emulation. Fig. 3(b) shows the decay in mean squared error (MSE) as time increases. It also clearly shows that the time required to reach a fixed MSE level increases as the size of the lattice increases. We define convergence time as the time required to reach an MSE level of 0.0025, which is equivalent to finding the time required to reach  $g - 0.05$  in Fig. 3(a) and was used to define convergence in [36].

**Averaging over samples from parallel runs to avoid autocorrelation:** We note that to get the *true* average convergence time of the p-bit network, we run each lattice emulation many times each time with different seed in random number generator and compute the average order parameter at each time point by taking an average of the absolute value of the order parameter calculated at the same time point from all the runs only. This allows us to eliminate the correlation between samples taken from the same run which yields longer convergence times and does not represent the actual convergence time of the network.

**Trotterization error:** In Fig. 2(c), we report the error in predicting the saturation value from using finite replica in our p-computer emulations. We compare our results against the 4q CT-PIMC algorithm developed in [36]. To ensure fidelity, we use the same C++ codes provided therein. With 10 replicas, we reproduce the CT-PIMC results with an absolute difference of 0.01 ~ 0.03 from the smallest to the largest lattice sizes. As reported in Ref. [36], we do not observe systematic changes in Trotter errors with lattice sizes.

#### IV. CLOCKLESS AUTONOMOUS OPERATION

In the last section, we have presented a digital implementation of a p-computer based on the graph-colored architecture. Even though it is not immediately obvious, we managed to use just two colors which happens to be the minimum number of colors possible and thus maximizes the number of p-bits that can be updated simultaneously. This allowed us to greatly reduce the convergence time compared to single flip Monte Carlo which updates just one p-bit at a given clock period and thus converges very slowly. However, there are two problems associated with this graph-colored digital implementation: first, a fully digital implementation of a p-bit requires thousands of transistors which increase the hardware footprint per p-bit quite significantly. This can be mitigated somewhat through the use of nano-magnet based compact p-bits which uses just three transistors and an MTJ. However, this also requires the use of digital to analog converters for each p-bit since the input to such compact p-bits is analog. The second issue with

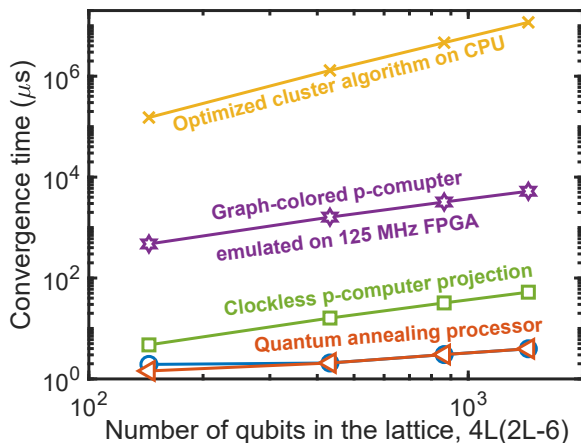


**FIG. 4. Comparing digital to clockless p-computer:** The clockless p-computer is simulated using SPICE, while the digital p-computer is estimated from MATLAB simulations assuming  $c \times f_c$  samples are collected every second,  $f_c$  being the clock frequency.

the digital implementation is that to perform colored update, all p-bits need to be synchronized through a global clock, the distribution of such clock throughout the chip becomes complicated with increasing number of p-bits and also slows down the frequency with which the system can be operated.

To circumvent the above issues, we next visit a fully analog implementation of p-computer with a clockless autonomous architecture. The clockless architecture is inspired from nature: natural processes do not use clocks. In clockless autonomous architecture, we do not put any restriction on the updating of p-bits. Each p-bit can attempt to update at any point of time without ever requiring a clock to guide them. Of course, errors will be incurred if two connected p-bits update themselves simultaneously and therefore with this scheme it is essential to minimize the probability of happening that. If there are  $d$  neighbors to each p-bit then the probability that two connected p-bit will update simultaneously is roughly  $d \times s^2$  where  $s = \tau_s / \tau_N$ ,  $1/\tau_N$  is the frequency with which a p-bit attempt to update itself and  $\tau_s$  is the time required to

propagate the information of a p-bit update to its neighbors. To make this clockless autonomous operation work it is essential to have  $s \ll 1$  (usually  $s \approx 0.1$  works well). This interesting possibility of clockless autonomous operation was introduced in [48] where a digital demonstration was made using FPGA. However, in this work we use a simple resistive synapse based architecture. Since resistors can instantaneously respond to the change in applied voltage, these type of synapse should be very fast compared to the average fluctuation time of s-MTJ based p-bits ( $\sim 100$  ps). We demonstrate the validity of this scheme by showing a SPICE simulation of a  $6 \times 6$  triangular AFM lattice with classical spins as shown in Fig. 4(a). As mentioned earlier, the triangular lattice is the base lattice of the square-octagonal lattice we have used so far. A partial view of the analog circuit simulated in SPICE which corresponds to the lattice above is also show in Fig. 4(d). We only show the resistive analog synapse providing the input for a single p-bit as marked. We use similar parameter values and same boundary conditions as we have used for the square-octagonal lattice



**FIG. 5. Time to solution for problems of increasing size using different hardware implementations:** The TTS is extracted using the protocol described in Fig. 3 for the problem defined in Fig. 2. The results for CPU and QA are from [36], while the results for the digital and clockless p-computers are obtained in this paper as described in the text.

(the same AFM coupling strength ( $|J_{AFM}| = 1$ ) inside the lattice and  $|J_{AFM}| = 0.5$  at the open boundaries). We also use the same definition for the order parameter. To keep it similar to what we have done in the previous section, we also use CCW initial condition in this example. Doing these help us to solve the problem in SPICE within a reasonable amount of time.

Fig. 4(b) shows the relaxation of the order parameter with time for the example described in Fig. 4(a). We use the same SPICE p-bit model used in [51]. We also show the relaxation curve obtained via a 3-graph-colored architecture (the triangular lattice in this example is 3 colorable). The graph-colored system as showing in Fig. 4(c) converges (based on the criterion we have used so far) around 72 samples. In 125 MHz FPGA that we have used earlier, this would take around  $72 \times 3 \times 8 \text{ ns} = 1.73 \mu\text{s}$ , whereas the corresponding analog circuit implementation converges in around 5 ns, converging around 400 times faster than similar digital implementation used earlier. Although the circuit used here is not programmable but it nicely illustrates the principle that around two orders of additional speed-up can be obtained with use of properly designed fully analog and clockless p-computer.

## V. RESULTS AND DISCUSSION

Finally, we show the time scaling for four different hardware in Fig. 5. We directly adopt the CPU and QA processor data from [36]. A simple curve fitting to CPU data reveals a roughly  $N_Q^2$  scaling where  $N_Q = 4L(2L-6)$  is the total number of qubits in the lattice. On the other hand, the p-computer results not only show a prefactor improvement but also an improvement in scaling compared to CPU. We observe an  $\sim N_Q$  scaling for p-

computer and as noted before, the reason for such a scaling improvement is due to the exploitation of massive parallelism where the number of p-bits that can be updated also increase with the lattice size (the scaling with number of p-bits is provided in Appendix F). Our results for the digital implementation of p-computer emulated on 125 MHz FPGA shows that for the largest lattice size ( $L = 15$ ) that has been emulated in [36], we should get a  $2000\times$  improvement over a single thread implementation on CPU. But it stands, the current FPGA emulations of our p-computer are  $\sim 3$  orders of magnitude worse than the physical quantum annealing processor. We expect another one order of magnitude improvement might be possible with these approach by using customized mixed signal ASIC design with s-MTJ based p-bits. However, based on the example of clockless operation shown in Section IV, we project another two orders of magnitude improvement in convergence time. This brings the gap with the quantum annealing processor down to one order or less. The operation of the quantum annealing processor might be governed by non-local quantum processes leading to the  $\sqrt{N_Q}$  scaling predicted in [52], though there are not enough data points to be certain.

## VI. CONCLUSION

In this work, we have presented a roadmap for hardware acceleration of QMC which is ubiquitously used in the scientific community to study the properties of many body quantum systems. We have mapped a recently studied quantum problem into a carefully designed autonomous probabilistic computer and projected 5-6 orders of magnitude improvement in TTS which is within a factor of 10 of what has been obtained from a physical quantum annealer. The massively parallel operation of a probabilistic computer together with the clockless asynchronous dynamics provides a significant scaling advantage compared to CPU implementation. Robustness, room-temperature operation, low power consumption and ultra-fast sampling – these features make it interesting to investigate the applicability of probabilistic computers to other quantum problems beyond the TFI Hamiltonian studied in this work.

## ACKNOWLEDGMENTS

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## AUTHOR CONTRIBUTION

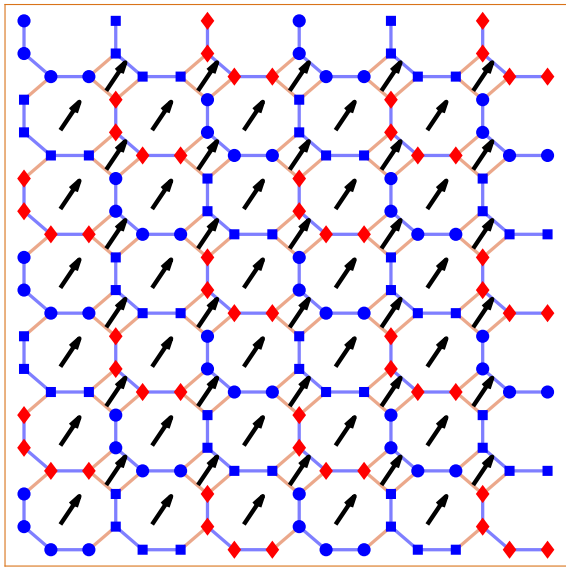
SC performed the simulations with help from KYC and wrote the first draft of the manuscript. All authors contributed to and participated in designing the experiments and editing the manuscript.

## COMPETING INTERESTS

One of the authors has a financial interest in Ludwig Computing. The authors declare no other competing interests.

### Appendix A: Appendix: CCW and Ordered initial states

Eq. (3) prescribed how to compute average pseudospin given a state of the qubits. Interestingly, we can carefully assign values to our qubits to get a configuration where the value of the average pseudospin is maximum. This occurs when all the triangular plaquettes inside this configuration align themselves in a particular direction as shown in Fig. 6 which gives it the name *ordered state*. The pseudospin value for this configuration is the maximum value for any square or octagonal plaquette i.e.,  $2/\sqrt{3}$ . We also note that this configuration is a ground state of a square-octagonal lattice of classical spins.



**FIG. 6.** A  $6 \times 6$  (144 qubits) 2D square-octagonal lattice in *ordered* state. All the plaquettes align themselves at an angle  $60^\circ$  with the horizontal axis. Note that there are six possible directions the plaquettes can align themselves to.

It is not the case that a ground state of the classical square-octagonal lattice always yields maximum value for pseudospin. It is also possible to have classical ground states for which the pseudospin value is zero (minimum).

Two examples of such states are CCW (counter clockwise) and CW (clockwise states) as shown in Fig. 7. The pseudospins of individual plaquettes for these configurations do not align themselves but rotate along the periodic boundary direction.

An interesting observation is that it is not possible to go to ordered state from these CCW and CW states just by making a local change in the configuration. The other way of saying is that these configurations are *topologically* protected. One needs to change all the spins simultaneously which also makes it difficult for algorithms which create samples by proposing local changes in the configuration of previous sample to quickly converge to the saturation value if the previous sample happens to be in one of these states.

### Appendix B: Appendix: More details of FPGA implementation

In this work, we define the operation of a p-bit using the following two equations:

$$\Delta E_i = m_i \sum_j W_{ij} m_j \quad (\text{B1})$$

$$m_i = -m_i \operatorname{sgn}(e^{-2\beta\Delta E_i} - r_{[0,1]}) \quad (\text{B2})$$

where  $j$  in Eq. (B1) runs through the set of the neighbors of  $i^{\text{th}}$  p-bit and  $r_{[0,1]}$  is a random real number uniformly distributed in  $[0, 1]$ . Eq. (B1) is known as the *synapse* equation and defines the input to the  $i^{\text{th}}$  p-bit. On the other hand, Eq. (B2) is known as the *neuron* equation and defines how a p-bit should change its state given the input. There is another well-known form of synapse-neuron equations in the literature which is:

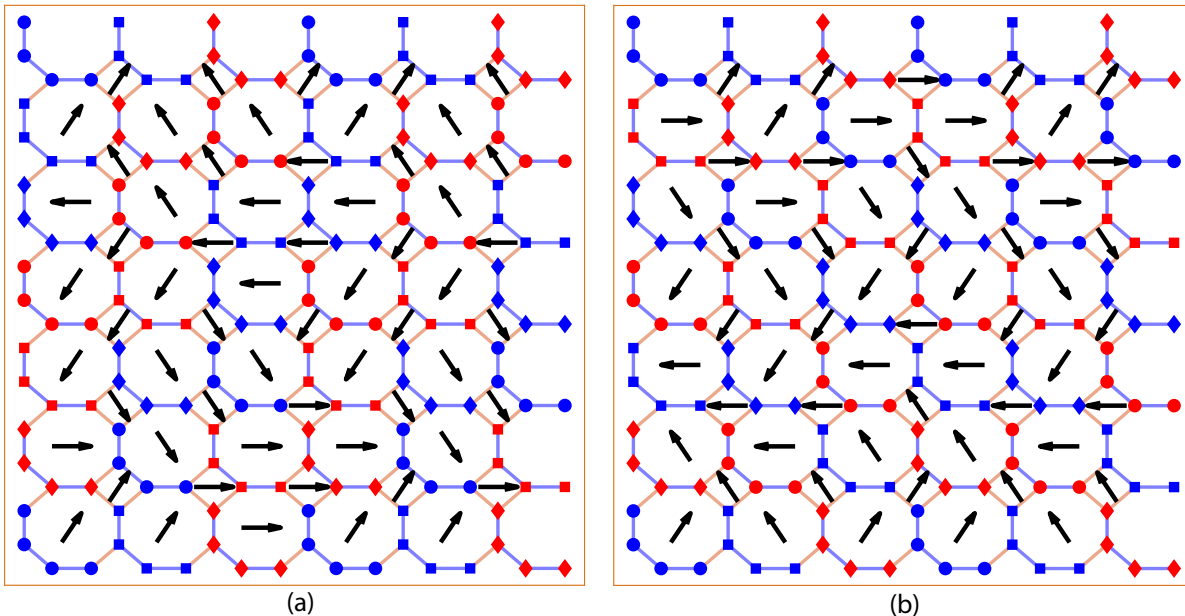
$$I_i = \sum_j W_{ij} m_j \quad (\text{B3})$$

$$m_i = \operatorname{sgn}(\tanh(\beta I_i) - 2r_{[0,1]} + 1) \quad (\text{B4})$$

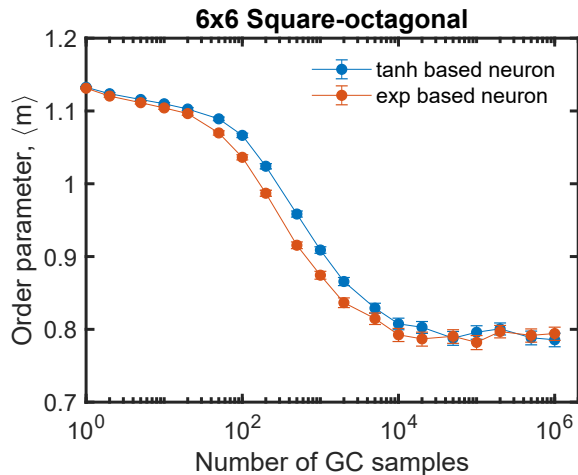
In our experiments, we have found that p-bit network with p-bits defined as in Eqs. (B1-B2) converges faster than those defined with Eqs. (B3-B4) as shown in Fig. 8 where we emulated the  $6 \times 6$  square-octagonal lattice starting from ordered initial condition.

The plot for  $6 \times 6$  lattice in Fig. 3(a) was generated from emulation of a graph-colored p-computer on FPGA (using Virtex<sup>®</sup> UltraScale+<sup>™</sup> - xcvu9p provided by AWS F1 instances and with a clock frequency of 125 MHz clock corresponding to 8 ns clock period). The p-bit network emulated in AWS FPGA follows a similar local weighted p-bit architecture proposed in [48], although we did not use the *autonomous mode*. Instead we used the graph coloring approach and was implemented by making use of local counters assigned with each p-bit which keep track of the p-bits to be updated based on their assigned color. In the qubit lattice, each qubit is connected to at most three other q-bits (except





**FIG. 7.** A  $6 \times 6$  (144 qubits) 2D square-octagonal lattice in (a) CCW and (b) CW states. The pseudospin of individual plaquettes rotates along the periodic boundary (vertical) direction. These two states leads to minimum value (zero) for average pseudospin.



**FIG. 8. Comparison between two types of neuron used for p-bit:** Performance comparison between p-bits described by Eqs. (B1-B2) and Eqs. (B3-B4). When emulating  $6 \times 6$  square-octagonal lattice, we see  $\sim 2\times$  improvement in number of samples require to convergence (as defined in this work) with the Eqs. (B1-B2).

for the qubits at the boundary along the horizontal direction, which are connected to either one or two other qubits). The p-bits in the translated network on the other hand, are connected to at most five other p-bits because of the replicas above and below. This allows us to design a fast and local synapse where at most only five inputs are to be considered. We use an activation function lookup table to mimic the operation of  $\exp(-2\beta x)$  function. We used 16-bit weight precision (1 bit for sign and 15 bits for value) along with Xoshiro128+ pseudo random

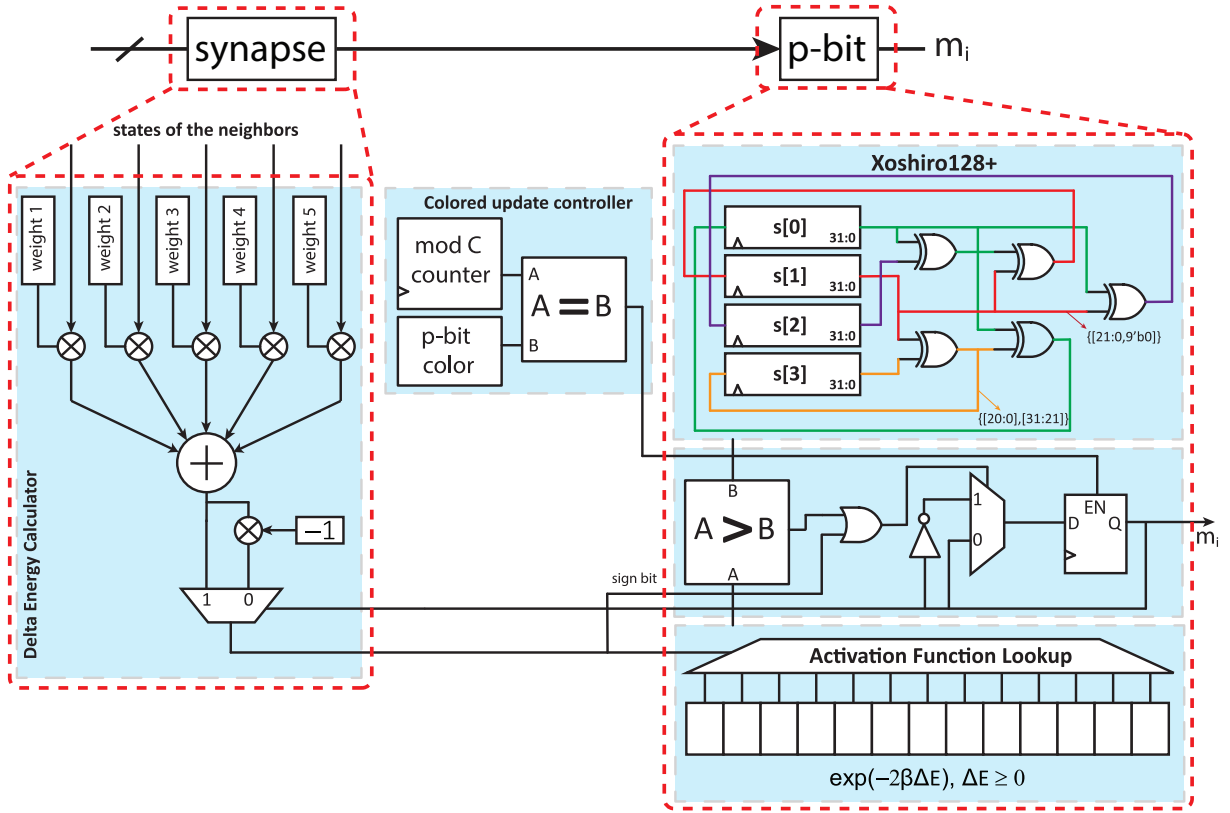
number generator (to perform accept-reject logic based on Metropolis-Hastings algorithm) which yielded visually similar quality samples as obtained from MATLAB<sup>®</sup> (where ‘mt19937ar’ random number generator was used) as evident from Fig. 10. In Fig. 3(a), only the smallest lattice was actually implemented in real AWS FPGA. Unfortunately, we did not have enough resources (see Table I for resource utilized for  $6 \times 6$  lattice) in AWS FPGA to emulate bigger lattice sizes but we expect that given enough resources our p-bit architecture would follow the projections made in Fig. 3(a). From Fig. 10, we can clearly see that the results from FPGA almost exactly follows the results from MATLAB<sup>®</sup>. To summarize, for next three larger p-computer curves, we project the time to convergence for other data points by (1) simulating the lattices on MATLAB<sup>®</sup>, (2) collecting number of samples required to converge (following the same criterion set in [36]), and (3) multiplying the number of samples from MATLAB<sup>®</sup> by 16 ns per sample.

**TABLE I.** FPGA resources utilized in the implementation of p-computer emulator for  $6 \times 6$  square-octagonal lattice.

	LUT usage	FF usage	BRAM usage	URAM usage	Power <sup>a</sup> (W)
<b>Absolute</b>	678534	567698	24.01	43	44.875
<b>%</b>	57.45	24.01	9.19	4.48	

<sup>a</sup> Estimated using Xilinx’s power estimation tool

We also note that it is possible to run multiple p-computers in parallel because they are relatively cheaper than quantum annealing processor which needs to con-



**FIG. 9. Simplified block diagram of a p-bit along with its synapse as implemented on FPGA:** The p-bit as defined in Eq. (B2) is modeled with three blocks on the right. The Xoshiro128+ [53] pseudorandom number generator on the top-right serves as the source of entropy. The activation function lookup on the bottom-right implements the exponential function for negative inputs. For positive inputs the p-bit is always flipped. The block in the middle-right serves as the comparator. The synapse on the left is modeled with an adder consisting of five inputs corresponding to five connections per spin in the replicated p-bit network. The output of the adder is multiplied by the current state of the p-bit and then passed to the activation lookup block of the p-bit. Finally, the colored updating of the p-bits is implemented by pre-assigning each p-bit a color value and adding a local counter with each p-bit. This counter increments at each clock pulses from the system clock and resets when the maximum color value is reached. When the local counter value becomes equal to the color value of the p-bit, only then the output of the p-bit is passed into the network. For simplicity, we did not show the system clock and other global control signals explicitly.

sume a large amount of power ( $\sim 25$  kW) for cooling. Using Xilinx power estimation tool to estimate the power consumed by the FPGA implementation of  $6 \times 6$  square-octagonal lattice (see Table I) we get  $\sim 45$  W for our implementation. Therefore at the same power consumption level 500 p-computer (consuming  $\sim 22.5$  kW power) could run in parallel giving 500 samples at each time point simultaneously yielding a significant improvement in *total* run-time of the problem. With the inclusion of nanomagnet based p-bits the power consumption for p-computer would go down even more. This should not be possible with QA processors because of their huge power consumption per machine for which they have to run these parallel runs sequentially.

### Appendix C: Appendix: Justification for using exponential fitting

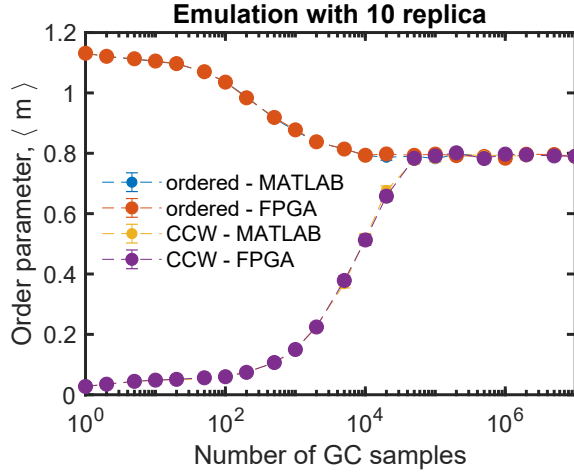
Initial probability vector,  $P_0$  is a  $N \times 1$  column vector where  $N = 2^n$  and  $n$  is the number of p-bits. Since, for every independent run, we start from a single state, therefore it has the following form:

$$P_0 = [0 \ 0 \ \dots \ 0 \ 1 \ 0 \ \dots \ 0]^T \quad (C1)$$

where the location of '1' corresponds to CCW (or any other fixed) initial state. Let  $W$  be our  $N \times N$  transition matrix and  $\lambda_0, \lambda_1, \lambda_2, \dots, \lambda_N$  are its eigenvalues in the descending order. Then  $\lambda_0 = 1$  and

$$P_0 = \alpha_0 |\lambda_0\rangle + \alpha_1 |\lambda_1\rangle + \alpha_2 |\lambda_2\rangle + \dots + \alpha_{N-1} |\lambda_{N-1}\rangle \quad (C2)$$

where  $|\lambda_i\rangle$  is the  $N \times 1$  eigenvector corresponding to eigenvalue  $\lambda_i$ . After applying  $W$  matrix for  $k$  times (which corresponds to running the emulator for  $k$  samples), we



**FIG. 10. Verification of FPGA emulation:** Emulation in FPGA is compared against the simulation in MATLAB to check the validity of the graph-coloring based FPGA implementation for ‘ordered’ and ‘CCW’ initial conditions. We could implement only the smallest lattice size ( $6 \times 6$  which corresponds to 144 qubits and 1440 p-bits) in the FPGA because of the unavailability of resources in FPGA. This plot shows that the FPGA results are in excellent agreement with MATLAB results. This also demonstrates the fact that both ordered and CCW initial condition lead to the same equilibrium value.

get the probability vector

$$\begin{aligned}
 P^{(k)} &= W^k P_0 \\
 &= \alpha_0 |\lambda_0\rangle + \alpha_1 \lambda_1^k |\lambda_1\rangle + \alpha_2 \lambda_2^k |\lambda_2\rangle + \dots \\
 &\quad + \alpha_N \lambda_N^k |\lambda_N\rangle \\
 &= \alpha_0 |\lambda_0\rangle + \alpha_1 e^{k \ln \lambda_1} |\lambda_1\rangle + \alpha_2 e^{k \ln \lambda_2} |\lambda_2\rangle + \dots \\
 &\quad + \alpha_N e^{k \ln \lambda_N} |\lambda_N\rangle
 \end{aligned} \tag{C3}$$

Now, the quantity  $m$  we are trying to evaluate has the form:

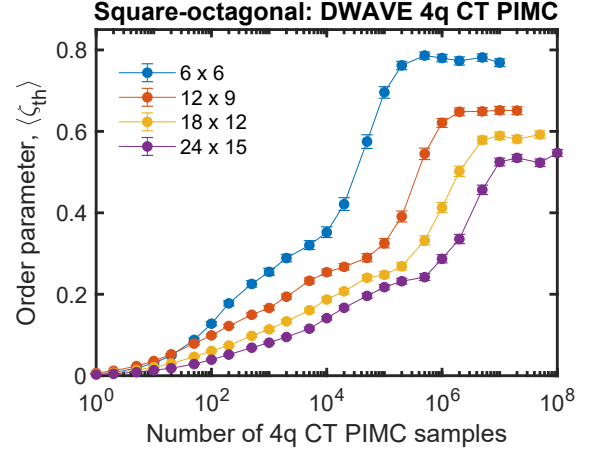
$$\begin{aligned}
 m &= \beta_0 p_0 + \beta_1 p_1 + \dots + \beta_N p_N \\
 &= \beta_0 (\alpha_0 \lambda_{00} + \alpha_1 \lambda_{01} e^{k \ln \lambda_1} + \dots + \alpha_N \lambda_{0N} e^{k \ln \lambda_N}) \\
 &\quad + \beta_1 (\alpha_0 \lambda_{10} + \alpha_1 \lambda_{11} e^{k \ln \lambda_1} + \dots + \alpha_N \lambda_{1N} e^{k \ln \lambda_N}) \\
 &\quad + \dots \\
 &\quad + \beta_N (\alpha_0 \lambda_{N0} + \alpha_1 \lambda_{N1} e^{k \ln \lambda_1} + \dots + \alpha_N \lambda_{NN} e^{k \ln \lambda_N})
 \end{aligned}$$

where  $\beta_i$  is the corresponding  $m$  value for the  $i^{\text{th}}$  state,  $p_i$  is the  $i^{\text{th}}$  element of  $P^{(k)}$  and  $\lambda_{ij}$  is the  $i^{\text{th}}$  element of eigenvector  $|\lambda_j\rangle$ . Rearranging, we get

$$\begin{aligned}
 m &= \alpha_0 (\beta_0 \lambda_{00} + \beta_1 \lambda_{10} + \dots + \beta_N \lambda_{N0}) \\
 &\quad + \alpha_1 (\beta_0 \lambda_{01} + \beta_1 \lambda_{11} + \dots + \beta_N \lambda_{N1}) e^{k \ln \lambda_1} \\
 &\quad + \dots \\
 &\quad + \alpha_N (\beta_0 \lambda_{0N} + \beta_1 \lambda_{1N} + \dots + \beta_N \lambda_{NN}) e^{k \ln \lambda_N}
 \end{aligned}$$

Therefore, we do expect that the output of the emulations to be a sum of many exponentials. In our experiments, we found that a fit with a sum of two exponentials

matches the data better than just a single exponential fitting.



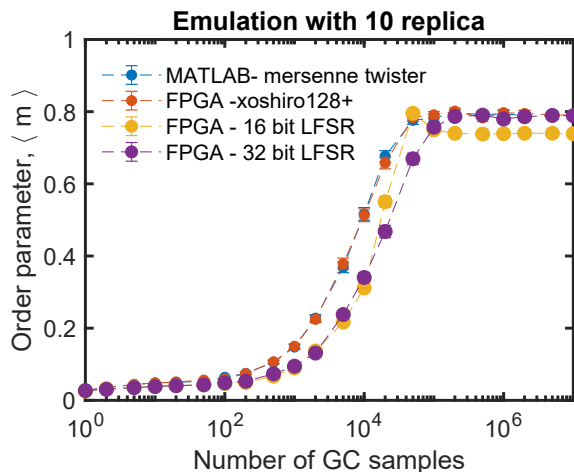
**FIG. 11. Equilibrium value determination:** We run the 4q-CT PIMC code provided by King et al. for all the four lattices and extract the equilibrium value. We use these values to calculate the errors in Fig. 2.

#### Appendix D: Appendix: Results from 4q CT-PIMC algorithm

We show the results of our simulation results with 4q CT-PIMC algorithm for all four lattice sizes in Fig. 11. Here we have defined one 4q-CT PIMC move as a sample. We fit these curves as described before and determine the equilibrium value. We use these results to compare the p-computer results in Fig. 2(c).

#### Appendix E: Appendix: Effect of the quality of random number generator

In this appendix, we also study the effect of the quality of random number generators for the benchmarking problem. Fig. 12, illustrates the importance of using high-quality random numbers. A cheap random number generator such as linear feedback shift register (LFSR) are not good enough. In software programs, one can generate very good random numbers using high quality RNG such as Mersenne twister but it requires many clock cycles to generate one random number. In hardware one can also generate moderately good quality random numbers (as shown in Fig. 12 xoshiro128+ works very well for this problem), but one needs to use too much digital footprint per RNG. The nano-magnet based ‘compact’ p-bits can provide a solution to both problem: it can generate true random numbers at a very high speed and requires very less hardware footprint.



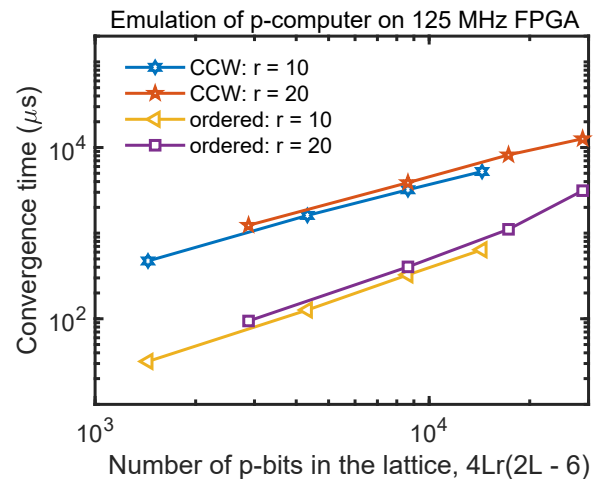
**FIG. 12. Effect of the quality of random numbers:**

The quality of random numbers are important for this benchmarking problem. Use of 16-bit LFSR per p-bit does not provide the correct saturation value. 32-bit LFSRs seem to reach the correct saturation value but take longer to converge. Use of costly but superior quality hardware RNG such xoshiro128+ provides excellent performance when compared with Mersenne-twister implemented on MATLAB. s-MTJ based compact p-bits can be useful for providing high-quality random numbers with high-throughput.

## Appendix F: Appendix: Scaling with p-bits

Finally we note that the scaling of convergence time with number of p-bits is actually  $\sim rN_Q$  for this problem when  $r$  is sufficiently large such that trotterization error is small. This has been shown in Fig. 13(a). The small differences in the curves for 10 and 20 replicas arise because they saturates at slightly different values (i.e., saturation values obtained using 10 replicas are more erroneous than saturation values obtained using 20 replicas). We also note that error with 4q CTPIMC reduces a little compared to 10 replicas when we use 20 replicas.

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**FIG. 13. Convergence time scaling with p-bits:** The scaling of convergence time with the number of p-bits in the lattice is shown for two different initial conditions. As can be seen here, the curves are almost linear yielding an  $Nr$  scaling with the number of p-bits. The small gap between two different replica sets can be attributed to their different saturation values.

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