# TAP: Accelerating Large-Scale DNN Training Through Tensor Automatic Parallelisation

Ziji Shi \*<sup>1,2</sup>, Le Jiang<sup>2</sup>, Ang Wang<sup>2</sup>, Jie Zhang<sup>2</sup>, Xianyan Jia<sup>2</sup>, Yong Li<sup>2</sup>, Chencan Wu<sup>2</sup>, Jialin Li<sup>1</sup>, and Wei Lin<sup>2</sup>

<sup>1</sup>National University of Singapore <sup>2</sup>Alibaba Group

# Abstract

Model parallelism has become necessary to train large neural networks. However, finding a suitable model parallel schedule for an arbitrary neural network is a non-trivial task due to the exploding search space. In this work, we present a model parallelism framework TAP that automatically searches for the best data and tensor parallel schedules. Leveraging the key insight that a neural network can be represented as a directed acyclic graph, within which may only exist a limited set of frequent subgraphs, we design a graph pruning algorithm to fold the search space efficiently. TAP runs at sub-linear complexity concerning the neural network size. Experiments show that TAP is  $20 \times -160 \times$  faster than the state-of-the-art automatic parallelism framework, and the performance of its discovered schedules is competitive with the expert-engineered ones.

# 1. Introduction

<sup>1</sup>Recent years have witnessed a burgeoning of large deep neural networks (DNNs) that deliver unprecedented accuracy across a wide range of AI tasks. In fact, the rate of DNN model size increase has far surpassed the growth in accelerator memory capacity. As a result, model parallelism has been proposed, where model weights are sharded onto multiple machines during distributed DNN training, to address this memory capacity issue.

There are two main paradigms in model parallelism: pipeline parallelism and tensor parallelism. Pipeline parallelism splits the model by layers. Only activations are communicated during the forward pass, while gradient tensors are exchanged in the backward phase. Pipeline parallelism has drawn much attention recently; many proposed algorithms attempt to find the optimal pipeline schedule that minimizes the pipeline idle time ("bubble size"). However, pipeline parallelism suffers from two significant drawbacks: 1) each layer has to be small enough to fit into a single accelerator's memory, and 2) if the model has an imbalanced architecture, interleaving different layers can be challenging. Tensor parallelism (or tensor sharding) is therefore proposed as an alternative. Tensor parallelism partitions the model weights and distributes them to multiple devices, lifting the restriction on single layer size.

Unfortunately, manual specification of tensor parallelism can be challenging and error-prone. The optimal partitioning scheme usually depends on both the neural network architecture and the hardware system. Prior approaches tightly couple user code, parallel strategies, and accelerator hardware, narrowing the adaptability of model parallelism in practice (e.g., cloud environment).

Can an optimal tensor parallel plan be found automatically? Existing work on automating model parallel training either rely on user hints or a brute-force search over the entire space. [14, 26] incorporate user annotations as hints to derive the pipeline or tensor sharding schedule, where users are required to specify the number of pipeline stages or the mapping between layer to physical device mesh. By inferring the full schedule based on expert knowledge, it was made easier to write parallel plans than manual specification [20, 24]. But the downside is that the manual specification may not generalize across different hardware topologies. [15, 33, 30] propose to search for the parallel schedule over a pre-defined search space. They leverage Dynamic Programming to find the best device placement for the shards of a neural network. However, the brute force search can be very slow in reality, as they need to deal with exploding search space. Modern neural networks can contain hundreds of thousands of operations, each having multiple possibilities of sharding. The search for the optimal tensor parallel plan can be reduced to the makespan problem. which has been proven to be NP-hard[16].

We argue that a brute-force search over the entire space is not necessary. We observe that 1) most neural networks contain shared subgraphs, which can be utilized to reduce search efforts when choosing parallel strategies, and 2) communication is the main bottleneck when training in tensor parallelism, and usually, it is impossible to overlap the contiguous partitions in a block using tensor parallelism. Therefore, we can drastically accelerate the search for better strategies by searching over unique neural network sub-modules only, and we should evaluate the candidate strategies with communication cost.

Based on those observations, we designed a system drastically reducing search space. Our contributions consist of the

<sup>\*</sup>ziji.shi@u.nus.edu

<sup>&</sup>lt;sup>1</sup>This paper was completed in October 2022.

following:

- A set of computational graph intermediate representations (IRs) that abstract away from the implementation details of low-level operations;
- A graph pruning algorithm that leverages the shared substructure to facilitate efficient searching;
- A communication-based cost model that accurately captures the amount of communication necessary in tensor-parallel training.

We present TAP, an deep learning framework that automatically derives a tensor-parallel plan for arbitrary neural networks without requiring expert annotations. TAP drastically reduces the search time using shared subgraphs, achieving  $20 \times -160 \times$  speedup in finding a competitive sharding plan. Evaluations show that our approach can find a comparable tensor parallel plan similar to an expert-designed solution.

# 2. Background

## 2.1. Data Parallelism

Data Parallelism is a commonly used parallel strategy that scales a model from a single worker to multiple workers by replicating the weights, as shown in Fig. 1b. Each worker maintains a full replica of the same model but trains on different data slices. In the forward pass, the workers compute the parameter updates independently on their own data slice, and different workers average the gradients through *AllReduce* to ensure that the model parameters of all workers are consistent during the backward pass.

## 2.2. Model Parallelism

Model parallelism is proposed to solve the downside of data parallelism: model weight has to be able to fit into the memory of a single accelerator. Model parallelism distributes the model weight into different devices and synchronizes the full model through collective communication[7]. Model parallelism can be divided into pipeline parallelism and tensor parallelism, depending on the point of view.

**2.2.1. Pipeline parallelism** Pipeline parallelism divides the model across the layers and distributes it to different devices[13, 19, 10], shown in Fig. 1c. In the forward pass, the training begins at GPU2, the data flows from GPU2 to GPU1 and finally reaches GPU0; the backward pass starts on GPU0, calculates the gradients, and updates the model parameters in the opposite direction to the forward pass. Pipeline parallelism aims to minimize device idle time. Ideally, the size of each layer should be similar so that each device's workload is relatively balanced during the training process. But in practice, the model architecture could be very heterogeneous, and the inter-device communication speed could differ significantly from inter-rack to intra-rack, thus greatly hindering the training speed.

**2.2.2. Tensor parallelism** Tensor parallelism splits the model layer and distributes it to different devices to disperse the

computational overhead of the layer[31, 27, 20], shown in Fig. 1d. For each device, only part of the input tensors are stored in its local memory, therefore the full result needs to be aggregated from partial results on other devices through collective communication. Tensor parallelism can alleviate the problem of training heterogeneous models using pipeline parallelism, and achieve better performance.

### 2.3. Automatic Parallelism

Automatic parallelism is a recent line of research on automatically distributing the local model from one device to multiple devices using the data and model parallel strategies. Existing works on automatic parallelism rely on user hints or bruteforce searches over the entire space.

**2.3.1. User hint** User-hint-based automatic parallelism is used to help users scale single-device programs to multi-device. For example, GSPMD[31] infers the operator partitioning scheme based on user annotations to scale single-device programs. Whale[14] allows for incorporating user hints to perform semi-auto parallelisation for large models and introduces a hardware-ware load balance algorithm. However, user-hint-based automatic parallelism approaches require users to have a deep understanding of both system and the model, and the hard-coded user hints may not be transferable when the model or system changes.

2.3.2. Search algorithm Recent work has proposed fully automatic approaches based on search algorithms to optimize distributed DNN training. For example, Tofu[30] uses a recursive search algorithm based on dynamic programming and DNN-specific heuristics to minimize communication for the entire dataflow graph. Flexflow[15] uses randomized search to find the best parallel strategy in the SOAP (Sample, Operator, Attribute, and Parameter) space. Alpa[33] optimizes large DL models through two-level optimizations: inter-operator and intra-operator. It automates inter-operator parallelism by dynamic programming and intra-operator parallelism by integer linear programming. Unity[28] represents parallelisation and algebraic transformations as substitutions on a unified graph representation, uses a novel hierarchical search algorithm to identify an optimized sequence of substitutions, and scales to large numbers of GPUs and complex DNNs.

**2.3.3.** Challenge of exploding search space The searchbased approaches face the challenge of exploding search space as model size scales, resulting in a huge time cost. Concretely, each tensor (assuming 2D) presents three possible sharding options: not sharding, sharding on the first dimension (rowwise), or sharding on the second dimension (column-wise). Given a neural network G(E, V) with V weight tensors, there exists  $3^V$  possible sharding plans. Therefore, there exists no polynomial time solution to find an optimal sharding plan.

# 3. Approach

In this section, we formulate the problem of searching for an optimal tensor parallel schedule, followed by our observation



of the common presence of shared sub-structures in a large neural network, leading to the motivation of our design.

#### 3.1. Problem Formulation

A neural network can be represented as a directed acyclic graph G(E,V) comprised of L layers. The set of vertices V represents the operators, and the set of edges E represents the data flow from producer to consumer operators. Operators can optionally carry a weight tensor. During the forward pass, an edge represents an activation tensor, while in the backward phase, it represents a gradient tensor. A layer  $L_i \in L$  is either a layer or a cluster of operators with a similar composition. Let the physical training system be S(m,n) where m is the number of worker nodes, and n is the number of accelerators per worker node. A parallel plan p is a new graph mathematically equivalent to G, but the order of nodes may change, and the communication node may be inserted into p. The cost function, Cost(p,S), measures training latency for a given plan and training system. The goal is to find an optimal parallel plan  $p^*$  where:

 $\begin{array}{ll} \underset{p}{\text{minimize}} & Cost(p,S)\\ \text{subject to} & p(X) = G(X) \forall X \end{array}$ 

How to find such a plan in an automated manner? Figure 2 illustrates the typical workflow of an auto-parallel system. The system first attempts to constrain the search space for splitting a model. With a more manageable search space, a search algorithm then produces one or more candidate plans for evaluation. All candidate plans are evaluated by a cost model that chooses the best plan with the lowest cost based on its evaluation criteria.

The end-to-end duration to produce an optimal schedule is a critical metric for an auto-parallel system. We identify three main factors that contribute to this overall completion time: the size of the search space, the time complexity of the searching algorithm, and the speed of the evaluation method.

#### 3.2. Challenges and Observations

As we see earlier, a major challenge faced by auto-parallel systems is the search space explosion problem. This exponential increase in candidate space has led to impractical search time



Figure 2: General recipe of automatic model parallelism frameworks.

to derive a parallel schedule for modern large models [33] (§ 6.3). It creates a dilemma: auto-parallel systems aim to accelerate large model training; however if *the derivation step itself* is too slow, it may offset the benefit of using an auto-parallel system.

How to effectively reduce this large candidate search space? To answer this question, we studied common scaling techniques for popular DNN models and summarized our findings in Table 1. We conclude that these techniques can be grouped into two major categories: scaling on the width by increasing the dimension of layers (e.g., adding the number of classes, adding attention heads, increasing the convolutional channels), or scaling on the depth by increasing the number of layers. Our key observation is that both techniques start with a *base subgraph*, i.e., a group of layers or operators, and expand from it. For instance, large-scale pre-trained language models such as BERT[8] and T5[22] consist of tens of transformer layers, and multi-class object classification networks like ResNet-50[12] are made of convolutional layers.

Furthermore, by analyzing expert-engineered parallel schedules ([20, 23, 24]), we observe that *parallel schedules are primarily identical for the same type of layers*. The underlying reason is that similar layers share a similar amount of computation and memory consumption. This has motivated us to explore the possibilities of reusing the parallel schedules discovered for the same layer to save search effort.

#### 3.3. Motivating Examples

We are motivated by two commonly encountered scenarios as depicted in Fig. 3: scaling along the width (a), or scaling along the depth (b). In an e-commerce setting, there exist

Scaling Technique	Task	Model	# Params	Shared Subgraph (SS)	# of SS
	Vision	ResNet50[12]	23M	Conv	$50 \times$
	Vision + Language	CLIP-Base[21]	63M	Transformer	12×
By width	Language Model	WideNet[32]	63M	MoE layer	$32\times$
	Vision	ViT-Huge[ <mark>9</mark> ]	632M	Transformer	$32\times$
	Vision	V-MoE[25]	15B	MoE layer	$24 \times$
	Speech	wav2vec 2.0[4]	317M	Conv, Transformer	$7 \times, 24 \times$
	Language Model	BERT[8]	340M	Transformer	$24 \times$
By depth	Language Model	T5-Large[22]	770M	Transformer	$24 \times$
	Language Model	GPT-3[5]	175B	Transformer	96×
	Language Model	Switch Transformer[11]	1571B	MoE layer	15×

Table 1: Shared subgraphs exist on many neural network models. "Conv" means convolutional layer, "MoE" means Mixture-of-Expert layer.



Figure 3: Motivating examples.

hundreds of thousands to millions of types of merchandise. Therefore, to classify a product image, a classification model like ResNet[12] must have a very wide fully connected (FC) layer. As shown in Fig. 3a, the size of the FC layer (205M floating point numbers) can be disproportionately larger than the feature extraction module (24M). In fact, the single gigantically wide layer can be too large to fit into an accelerator, therefore, preventing the use of pipeline parallelism.

Another scenario is the family of models built using dense transformer architecture as shown in Fig. 3b. Transformer[29] has been the building block for many large language models (Table 1). A typical transformer layer comprises a self-attention and a multi-level perception (MLP) layer. The self-attention layer has 4 weight tensors Q, K, V, W, and the MLP layer has 2 weight tensors: one for the *intermediate* layer and one for the *output* layer. A dense transformer model usually scales up by stacking transformer layers [8, 22, 5, 9]. Due to the similarity in model architecture, we may reuse the sharding plan found for one layer on all transformer layers[20].

Under both scenarios, tensor parallelism proves to be a more general solution, which has motivated us to formulate the problem under a unified view.

#### 3.4. Split-Replica-Communication (SRC) Abstraction

Inspired by the observation that heavy bulky matrix multiplications of tensors drive model parallelism, TAP uses a unified view to represent a data and tensor parallelism schedule using the SRC abstraction.

**Split(axis).** *Split* means sharding the tensor on a target axis, and different device stores different partitions. Under this view, data parallelism is a special case for tensor parallelism where the tensor shards on the first dimension (batch dimension).

**Replica.** *Replica* means to replicate the tensor on different devices without sharding. For example, in data parallelism, the model tensors are replicated while the input tensors are sharded.

**Communication.** Splitting results in partial values. Also, the back-propagation requires aggregating different copies of gradients. Therefore, additional communication operators may be required to combine the partial results to ensure mathematical equivalence.

It is worth noting that we are not required to use all S&R&C. We may have patterns expressed as *R*-only, S&C, R&C, or S&R&C. Under the SRC abstraction, the original operator expression

$$Y = Op(A, B)$$

will be converted to a distributed version by

$$SR(Y) = Comm(Op(SR(A), SR(B)))$$

With the SRC abstraction, we can define general sharding rules for each operator. They are implemented as *ShardingPatterns* in TAP. If there is no viable way to split, we can always fall back to replicating the tensors (data parallel).

Fig. 4 illustrate a matrix multiplication (MatMul) pattern in TAP under SRC abstraction. X and W are 2D matrices, representing input tensor and weight tensor respectively. X is sharded column-wise while W is sharded row-wise.  $X_0$  and  $W_0$ are stored on device 0. Notice that standard MatMul still works for the sharded tensors, hence  $Y_0$  shares the same shape as Y. However,  $Y_0$  is just a partial result, and it needs to be added with  $Y_1$  from device 1 to get Y. As such, an AllReduceSum communication is required to sum them up for mathematical equivalence.



Figure 4: Example using SRC abstraction to perform MatMul on two sharded tensors. Only *S&C* were used.

# 4. Design and Implementation

#### 4.1. Overview

As depicted in Fig. 5, given a neural network represented as a graph, TAP first converts the graph into its intermediate representation(§ 4.2) called GraphNode and removes auxiliary nodes. Then TAP performs graph pruning(§ 4.3), restricting the search space from the complete graph to the subgraphs instead. After pruning, TAP explores the possible sharding opportunities using pre-defined sharding patterns(§ 4.4) and validates the candidate plans(§ 4.5). If a valid plan is found, it is then evaluated using the cost model(§ 4.6). In the end, TAP takes the best plan, performs additional optimizations on communication, and rewrites the model into a parallel version(§ 4.7.1).

Example 1: Auto-parallel code with TAP on 2 workers each with 8 GPUs

```
1 import tensor_auto_parallel as tap
2 mesh = [2, 8]
3 tap.auto_parallel(tap.split(mesh))
4 model_def()
```

## 4.2. Intermediate Representation

TAP defines a family of high-level Intermediate Representations (IRs) to facilitate the derivation of parallel schedules. Compared to MLIR HLO[17], TAP IRs operate on a coarser granularity while preserving the necessary information for sharding.

Upon obtaining the original neural network graph, TAP first trims the graph by deleting the auxiliary operators (Step (1) in Fig. 5). This will remove the initialization and checkpoint-related operators, which will be recovered when converted

back to a neural network graph later. As a result, the remaining graph will consist of only computing and communication operators.

TAP IRs consists of:

**GraphNode.** A GraphNode represents a group of computing or communication operators. It can be a layer or a logical group of operators, which is the basic unit for deriving the sharding schedule. The TAP graph is made of GraphNode while preserving the directed edges from the original DAG. Using the GraphNode IR, we reduce the number of nodes in the T5-large model from 60k to 1015 weight variables.

**Sharding pattern.** A GraphNode could have multiple ways of sharding. For instance, a 2D matrix weight can be split on either dimension or replicated. TAP defines each sharding pattern using the SRC abstraction. TAP also establishes the cost of each sharding pattern based on communication cost.

**Sharding plan.** A sharding plan is a set of subgraphs (blocks of GraphNodes) with sharding patterns connecting them.

# 4.3. Pruning using Shared Subgraph

It is common for DNN models to contain shared subgraphs. If we could identify the shared subgraphs, we could prune the search space by searching only within the subgraph. We propose a graph pruning algorithm to compress the search space into a shared structure (Step (2)):

## Algorithm 1 Graph Pruning

1:	<b>procedure</b> PRUNEGRAPH( <i>modelDef</i> , <i>minDuplicate</i> )
2:	$nodeTree \leftarrow \emptyset$
3:	$maxDepth \leftarrow modelDef.depth$
4:	for all $depth \in maxDepth \cdots 1$ do
5:	$nodeTree[depth] \leftarrow$
	longestCommonPrefix(modelDef.nodes.name)
6:	opCount = findSimilarBlk(nodeTree[depth])
7:	if $opCount \geq minDuplicate$ then
8:	subgraphs.append(nodeTree[depth])
9:	else
10:	break
11:	end if
12:	end for
13:	<b>return</b> subgraphs
14:	end procedure

In deep learning frameworks like TensorFlow[3], each variable is referred to by the operator that produces it. As such, variables under the same layer share the same name scope because they receive input from the same operator. Therefore, it is possible to cluster operators that fall under the same name scope.

Algorithm 1 starts by constructing a *nodeTree*, which identifies and groups the GraphNodes on each level by using the



Figure 5: Overview of the TAP system.

longest common prefix algorithm on the GraphNodes names (line2-5). After that, it finds the blocks of GraphNodes with a similar composition of operators and compares the number of operators with the minimum duplicate threshold (line 7). As the depth decreases, we will see a larger subgraph with less homogeneous compositions. Notice that multiple shared subgraphs may exist since a neural network may have multiple leaf nodes.

# TAP only needs to work on hundreds of plans thanks to pruning. However, not every plan is valid because we only have weekly connected subgraphs. Therefore, the candidate plans need to be validated by checking the connectivity (line 5-10). Upon checking, TAP evaluates the performance of each plan using a cost model and selects the best plan.

# 4.5. Pattern Routing

In the *pattern routing* step (Algorithm 3), TAP tries to assemble the weakly connected GraphNodes into a valid sharding plan by checking the connectivities. This is to ensure the success of graph rewriting (Step (5)). TAP does so using breadth-first-search (BFS) starting from the root node, and the goal is to make sure there exists at least a connected path from

# 4.4. Sharding Plan Generator

Alg	Algorithm 2 Derivation of Optimal Plan				
1:	<b>procedure</b> DERIVEPLAN(modelDef, shardingPatterns)				
2:	$subgraphs \leftarrow PruneGraph(modelDef)$				
3:	$candidatePlans \leftarrow enumerateAllPlans(subgraphs)$				
4:	$validPlans \leftarrow \{\}$				
5:	for all $p \in candidatePlans$ do				
6:	validated $\leftarrow$ PatternRouting(p)				
7:	if validated then				
8:	validPlans.insert(p)				
9:	end if				
10:	end for				
11:	$bestPlan \leftarrow min(QueryCost(validPlans))$				
12:	<b>return</b> best Plan				
13:	end procedure				

A sharding pattern, defining the way a GraphNode can be sharded, also serves as the directed edge between nodes. According to the SRC abstractions, the communication pattern is determined once the split/replica decision is made. Under the hood, the sharding patterns connect to each other like a chain.

After pruning, TAP proceeds to derive the optimal plan (Step(3) and (4)) using Algorithm 2. In the first phase, TAP enumerates all possible sharding plans given the subgraphs.

the root to the leaf chained using the sharding patterns.

One challenge is that a pair of contracting sharding patterns may have different input and output tensors, and a consumer operator's input is not ready until its producer is ready. In other words, dependencies exist between GraphNodes, but the information was kept in the original edges and could be lost when we perform pruning.

To solve it, we perform a topological search for the GraphNode based on the readiness of the input tensor. We leverage that neural networks can be represented using a directed acyclic graph, and reconstruct the edges based on the order of the producer-consumer relationship. This way, TAP avoids checking the order for every pair of GraphNodes.

#### 4.6. Cost Model

To build a cost model, we first profile different tensor parallel plans to understand the bottleneck. Fig. 6 summarizes the result. Data were collected from two nodes interconnected by 32 Gbps Ethernet, each equipped with 8 GPUs. We observe that *inter-node communication is the main bottleneck for tensor parallelism*, and *the best plan is not necessarily the one that splits every weight tensor*, in line with [7].



Figure 6: Time breakdown for tensor parallel plans on T5-large model on 8 and 16 GPUs (8w/16w). DP means data parallel, MHA means sharding the multi-head attention, FFN means sharding the feed-forward layer, and Megatron refers to the tensor sharding plan described in [20].

As the number of devices increases from  $8 \times$  to  $16 \times$ , the difference between communication time and computation time is further pronounced. This is because the bottleneck has shifted from high-speed intra-node communication (PCI-e) to slower inter-node communication (Ethernet).

Furthermore, the best tensor parallel plan for 16 GPUs (*16w-FFN*) only shards the weight in the feed-forward layer. We conjecture that with more tensors split instead of replicated, there are fewer FLOPs per device and the computation time is lower. However, this comes at the cost of having more communication. In the case of training in the data center where

nodes are interconnected by Ethernet, the speed bottleneck may shift from computation to communication instead. Therefore, communication cost is the main consideration when we design the cost model.

Motivated by the two observations above, TAP adopts the amount of communication as the cost of each plan. But calculating the correct amount of communication is not straightforward, as there exists a few practical challenges as below:

**Counting communicated parameter.** Although the amount of FLOPs is mostly symmetrical between the forward and backward phases, their communication patterns differ. During the forward phase, all activation tensors will be communicated, yet DNN frameworks will only communicate *non-constant* parameters during the backward phase. Therefore, the TAP cost model should be able to identify the weight that requires communication.

**Gradient overlap/aggregation.** The communication/computation patterns are different in the forward and backward phases. During the forward phase, the computation of the current layer is blocked until the input arrives from the previous layer, creating the temporal dependency. However, the communication during the backward phase can be overlapped with computation because the weight update stage is independent of gradient communication.

Furthermore, a large fraction of weights in a neural network are small tensors of tens to hundreds of bytes, but collectively they cause a large number of communications. To reduce the overhead of sending many small gradient packets, TAP fuses multiple gradients into one and overlaps with computation during the graph rewriting phase(§ 4.7.1). As a result, the amount of gradient communication may not fully translate into communication time in the backward phase.

Efficiency of collective communications. We observe that the communication efficiencies are different for different collective communication. For instance, we observe that AlltoAll and AllGather take more time to communicate the same amount of messages compared to the heavily optimized AllReduce in NCCL.

TAP addresses these issues using an analytical cost model based on the tensor's communication method, shape, and data format. Each sharding pattern is associated with a cost, and the total cost is calculated by summing all pattern costs along the critical path.

### 4.7. Graph Rewriting

After evaluating the cost of each sharding plan, TAP assembles the parallel plan. It does so by first restoring the original order of operators. Then, TAP identifies optimization opportunities that can be performed through gradient packing. In the end, TAP passes the resulting parallelized neural network plan to the deep learning framework runtime.

**4.7.1. Gradient packing.** TAP optimizes communication by packing multiple small gradient updates into a larger one

during the gradient synchronization stage, saving the communicator setup overhead. During the backward pass, each layer produces gradients that will be synchronized with other workers. This can be very time-consuming, as the number of gradient packets sent equals the total number of trainable parameters in a neural network.

As a communication optimization technique, TAP fuses packets smaller than a threshold  $\mu$  into one larger one. To prevent the aggregated packet from growing too large and deferring the weight update stage, TAP segments the packets into equally sized chunks. Therefore, the gradient synchronization and weight update stages can be pipelined, allowing the former to transmit while updating the weight parameters.

## 4.8. Limitation and Future Work

To further optimize the memory consumption, TAP could leverage other orthogonal techniques such as Auto Mixed Precision (AMP) [1], recomputation [6], and pipeline parallelism. Since both AMP and TAP optimize on the graph representation of the neural network, they can be made into different passes. Also, gradient checkpointing can be used to offload the selected GraphNode onto the main memory. TAP may also be used with pipeline parallelism through automatic[19, 18, 10, 14] or manual placements.

# 5. Complexity Analysis

This section presents an in-depth analysis of the arithmetic complexities of known algorithms in auto-parallelism.

## 5.1. Complexity Analysis of Existing Solutions

Following the discussion on related work, we analyze the complexities of two automatic model parallel frameworks and present it in Table 2. We define the total complexity as:

5.1.1. FlexFlow. FlexFlow operates on four dimensions (S/O/A/P), and there was no space reduction. Therefore, the search space is N(4E, 4V). As search complexity, FlexFlow employs the Markov chain Monte Carlo (MCMC) algorithm. Thus, we use B to denote the number of trials in MCMC sampling. Furthermore, within each trial, it needs to evaluate its performance by querying the cost model with Depth-First-Search(DFS), hence its evaluation complexity is O(V + E). 5.1.2. Alpa. Alpa is formulated as a multi-level optimization problem: in the outer loop, it searches for the inter-op plan using dynamic programming; in the inner loop, it finds the intra-op parallel plan using integer linear programming. First, since it operates at MLIR HLO, which is a finer IR than the TensorFlow operator, we formulate the search space as N(kE, kV) where k > 1. In the outer loops, it uses a similar algorithm to [18] to search for pipeline slices and map the slices



Figure 7: Tuning minDuplicates for Algorithm 1

to devise mesh. Optimization like operator clustering and early pruning reduces the outer loop complexity to  $(kV)^2L$ . For the inner loop, since the exact complexity of their ILP solver is unknown, we use a lower bound by performing a BFS from each operator, and the complexity is given as kE(kV + kE). Finally, each trial needs to evaluate its performance by querying the cost model, so the evaluation complexity is kV + kE.

**5.1.3. TAP**. In TAP, we first reduce the search space by converting the TensorFlow graph to TAP graph (by  $C \times$ , where  $C \ge 1$ ). We then prune the tree by layer, further reducing the complexity to  $N(\frac{E}{2CL}, \frac{V}{2CL})$ . In the searching stage, the result is derived by performing a BFS. Thus, the complexity is  $\frac{V+E}{2CL}$ . For the evaluation stage, TAP needs to evaluate the cost of each plan by querying the cost model, which depends only on the size of the edges. Thus, the evaluation cost is  $\frac{E}{2CL}$ .

# 6. Evaluation

## 6.1. Setup

We first evaluate the pruning algorithm and the use of Just-In-Time compilation for TAP. Then, for comparison with another auto-parallel framework, we use Alpa version 0.7 running with JAX 0.3.5. Next, we use Megatron running on PyTorch to compare against expert-engineered tensor parallel plans. Finally, we present the training convergence running gigantic neural networks.

The evaluation was performed on Company A's public cloud node with 756GB main memory,  $2 \times$  Intel 8163 CPUs at 24 cores each, and  $8 \times$  Nvidia V100 SXM2 32GB GPUs. Additionally, TAP builds on top of TensorFlow 1.12.

#### 6.2. Micro Benchmarks

**6.2.1. Pruning Algorithm** One of the key contributions of TAP is the graph pruning algorithm, in which minDuplicates determines the minimum size of subgraphs. If the threshold for subgraphs is too low, we may still face exploding search spaces; if the threshold is too high, we may see too few subgraphs, resulting in a longer search time. Since

Framework Search Space		Search Algorithm	Evaluation	Total
FlexFlow	N(4E, 4V)	В	O(V+E)	O(BV + BE)
Alpa	N(kE,kV)	Inter-Op: $O(V^2L)$ Intra-Op: $O(E(V+E))$	O(V+E)	$O(V^2L(V+E^2))$
ТАР	$N(\frac{E}{2CL}, \frac{V}{2CL})$	$O(\frac{E+V}{L})$	$O(\frac{E}{L})$	$O(\frac{E+V}{L})$

Table 2: Complexities of selected auto model parallel frameworks.



Figure 8: Training time per iteration when XLA is enabled. Lower is faster.

the architecture of different neural networks may vary significantly, it is desirable to have a robust threshold.

We explore a range of minDuplicates and report the number of unique subgraphs found and graph pruning algorithm runtime in Fig. 7. We conclude that the threshold is robust and does not require significant effort in tuning. Take the T5large model with 770M parameters as an example. When the threshold is 1, meaning the graph is unpruned, it contains 6561 nodes. After pruning, the number has been drastically shrunk to just 5. As the threshold changes, the number of identified unique blocks stays relatively stable, showing that our graph pruning algorithm is insensitive to different thresholds.

Furthermore, we observe that the pruning algorithm is very efficient, taking less than 12 seconds to find the subgraphs for T5-large, and less than a second for the 152-layer 100K-class ResNet model, which proves the scalability of TAP's graph pruning algorithm.

**6.2.2.** XLA XLA[2] is a JIT compiler for DNN frameworks, optimizing the training mainly through fusing smaller kernels to reduce launch overhead. Like TAP , XLA identifies the connected subgraphs and optimizes on the operator level. We evaluate the time per iteration with and without XLA on the ResNet50 model with varying numbers of classes. Fig. 8 shows that the improvement from XLA is not consistent, and we observe a similar trend in T5 models, which has performance improvement between -9% to +1%. We believe the inconsistent performance improvement results from new communication nodes being inserted into the parallelised plans by TAP . Therefore, XLA may have difficulty identifying the correct cluster of operators to fuse. Furthermore, XLA's oper-

ator clustering may hinder the degree of communication and computation overlap, affecting the scaling efficiency. For this reason, we did not enable XLA for the rest of the experiments.

### 6.3. End-to-End Evaluation

In this section, we compare with auto-parallel framework Alpa on search time and performance of the discovered plan.

**6.3.1. Search time.** As explained in § **5.1**, TAP has a sublinear time complexity, which is desirable when the models' size scales up. In the experiments with Alpa, we present the end-to-end search time with respect to model scaling, defined by the duration from the start of the experiment till the moment that the training process begins. Due to time constraints, we shortlisted a search space of 16 plans for T5 and 5 plans for ResNet, while we did not restrict the search space for TAP.



Figure 9: End-to-end search time when scaling on the number of parameters for dense transformer model.

To scale the model along the depth, we increase the number of transformer layers for T5, an encoder-decoder transformer architecture for language modeling. Increasing the depth of dense transformer models is a common practice to improve performance. Fig. 9 shows that, with rising parameters, TAP can still find a plausible schedule in under 15 mins, which is  $21 \times -67 \times$  faster than Alpa.

To scale the model size along the width for the ResNet50 model, we choose to increase the size of the classification layer. The original ResNet50 model has 1024 classes in the classification layer. As we increase the dimensions for the classification layer, the total number of parameters also scales up. As shown in Fig. 10, TAP is two orders of magnitude



Figure 10: End-to-end search time when scaling on the number of parameters for the large-scale classification model.

faster than Alpa in finding the optimal solution. Our systems outperforms it by  $103 \times -162 \times$ .

We further analyze the time breakdown during the search. For example, for 24-layer T5-large (770M parameters), Alpa spent 5 mins profiling the operators and 5 mins constructing the pipeline stages out of the operators. Instead, TAP reduces the architecture to one transformer block and searches for shardable parameters within that only, drastically reducing the search space. As a result, Alpa takes 197 minutes to search for 16 candidate plans, while TAP requires only 6 minutes to examine 729 candidate plans.



Figure 11: Training time per iteration for T5 (batch size=16). The blue band represents the standard derivation.

**6.3.2. Training speed.** We also evaluate the performance of the best plans produced by Alpa and TAP. We observe that Alpa favors pipeline parallel schedules, while the optimal schedule found by TAP is similar to the Megatron-style tensor parallel schedule. Since the plans using pipeline parallelism require less communication, the plans from Alpa have a higher throughput.

We also observe that as the width of the model increases, the performance of TAP plans is better and more consistent.



Figure 12: Training time per iteration for ResNet50 (batch size=1024).



Figure 13: Comparison between TAP and Megatron plan.

Fig. 12 shows the time to finish one iteration of training for parallel plans of ResNet50. We first observe that TAP consistently outperforms Alpa. Further, the variance (blue band) in plans discovered by Alpa shows that it struggles to find consistently good plans.<sup>2</sup>

## 6.4. Evaluation of Optimal Sharding Plan

We compare the best parallel plan found by TAP with an expert-engineered plan described in [20]. Megatron runs on PyTorch.

**6.4.1. Memory and training speed.** We observe from Fig. 13 that the best parallel plan found by TAP is more memory efficient than Megatron, making it more scalable for large neural network models since the memory capacity is usually the bottleneck. Furthermore, regarding training speed, TAP's best plan is only within 2.3% to 14.8% slower than the Megatron plan.

**6.4.2. Visualization of discovered plans.** We plot some of the sharding plans discovered by TAP in Fig. 14. For dense

 $<sup>^2\</sup>mathrm{TAP}$  only outputs the best plan out of all possible plans. Therefore it only has one line.



Figure 14: Selected sharding plans discovered by TAP for T5. Each box represents a trainable variable in the transformer layer.

transformer models, we observe that TAP usually shards the weight variable in the multi-head attention layer while keeping the embedding and layernorm layers replicated. Therefore, we conjecture that the attention and FFN layers are usually more parameter-heavy, making them more suitable for weight sharding.

We also found that TAP was not only able to discover Megatron-style fully sharded plans or data-parallel plans but also can it find partially sharded plans that only split multihead attention (*MHA-only*) or feed-forward layers (*FFN-only*). To our surprise, the best plan found by TAP on the experiment system is the FFN-only plan, where the multi-head attention (green) gets replicated, and the feed-forward layer (yellow) is sharded. Unlike fully sharded plans like Megatron, the FFNonly plan will make more efficient use of the available GPU memory and save commutation when GPU resource is abundant so that it does not need to aggregate the partial activations in the forward pass.

## 6.5. Scaling beyond Single Worker

To push the boundary of the scalability, we train the 100 billion parameters M6-MoE-100B model with 128 NVIDIA V100 GPUs and 1 trillion parameter M6-MoE-1T with 480 NVIDIA V100 GPUs. We scale model parameters by ten times while only increasing GPU count by 3.75 times. Besides the resource saved per parameter, M6-MoE-1T showed a significant model quality gain compared to M6-MoE-100B, as shown in Fig. 15.



Figure 15: Training loss of M6-MoE-100B and M6-MoE-1T.

# 7. Conclusion

We present TAP, an automatic parallelism framework that efficiently discovers data/tensor parallel plans for large models. Leveraging the observation that shared subgraphs widely exist in neural networks, we design a pruning algorithm and SRC abstraction that efficiently reduces the search space with a sublinear end-to-end complexity. The best plans found by TAP are comparable with the state-of-the-art expert-engineered plans while only taking minutes to discover. TAP will be open-sourced on GitHub.

# References

- Automatic mixed precision for deep learning. https://developer. nvidia.com/automatic-mixed-precision.
- [2] XIa: Optimizing compiler for machine learning. https://www.tensorflow.org/xla.
- [3] Martín Abadi, Ashish Agarwal, Paul Barham, Eugene Brevdo, Zhifeng Chen, Craig Citro, Greg S. Corrado, Andy Davis, Jeffrey Dean, Matthieu Devin, Sanjay Ghemawat, Ian Goodfellow, Andrew Harp, Geoffrey Irving, Michael Isard, Yanqqing Jia, Rafal Jozefowicz, Lukasz Kaiser, Manjunath Kudlur, Josh Levenberg, Dan Mane, Rajat Monga, Sherry Moore, Derek Murray, Chris Olah, Mike Schuster, Jonathon Shlens, Benoit Steiner, Ilya Sutskever, Kunal Talwar, Paul Tucker, Vincent Vanhoucke, Vijay Vasudevan, Fernanda Viegas, Oriol Vinyals, Pete Warden, Martin Wattenberg, Martin Wicke, Yuan Yu, and Xiaoqiang Zheng. TensorFlow: Large-Scale Machine Learning on Heterogeneous Distributed Systems. 2016.
- [4] Alexei Baevski, Yuhao Zhou, Abdelrahman Mohamed, and Michael Auli. wav2vec 2.0: A framework for self-supervised learning of speech representations. Advances in Neural Information Processing Systems, 33:12449–12460, 2020.
- [5] Tom Brown, Benjamin Mann, Nick Ryder, Melanie Subbiah, Jared D Kaplan, Prafulla Dhariwal, Arvind Neelakantan, Pranav Shyam, Girish Sastry, Amanda Askell, et al. Language models are few-shot learners. Advances in neural information processing systems, 33:1877–1901, 2020.
- [6] Tianqi Chen, Bing Xu, Chiyuan Zhang, and Carlos Guestrin. Training deep nets with sublinear memory cost. arXiv preprint arXiv:1604.06174, 2016.
- [7] Jeffrey Dean, Greg S. Corrado, Rajat Monga, Kai Chen, Matthieu Devin, Quoc V. Le, Mark Z. Mao, Marc Aurelio Ranzato, Andrew Senior, Paul Tucker, Ke Yang, and Andrew Y. Ng. Large scale distributed deep networks. Technical report, 2012.
- [8] Jacob Devlin, Ming Wei Chang, Kenton Lee, and Kristina Toutanova. BERT: Pre-training of deep bidirectional transformers for language understanding. Technical report, 2019.

- [9] Alexey Dosovitskiy, Lucas Beyer, Alexander Kolesnikov, Dirk Weissenborn, Xiaohua Zhai, Thomas Unterthiner, Mostafa Dehghani, Matthias Minderer, Georg Heigold, Sylvain Gelly, et al. An image is worth 16x16 words: Transformers for image recognition at scale. arXiv preprint arXiv:2010.11929, 2020.
- [10] Shiqing Fan, Yi Rong, Chen Meng, Zongyan Cao, Siyu Wang, Zhen Zheng, Chuan Wu, Guoping Long, Jun Yang, Lixue Xia, Lansong Diao, Xiaoyong Liu, and Wei Lin. DAPPLE: A pipelined data parallel approach for training large models. *Proceedings of the ACM SIG-PLAN Symposium on Principles and Practice of Parallel Programming, PPOPP*, 21:431–445, 2021.
- [11] William Fedus, Barret Zoph, and Noam Shazeer. Switch transformers: Scaling to trillion parameter models with simple and efficient sparsity, 2021.
- [12] Kaiming He, Xiangyu Zhang, Shaoqing Ren, and Jian Sun. Deep residual learning for image recognition. In *Proceedings of the IEEE Computer Society Conference on Computer Vision and Pattern Recognition*, volume 2016-Decem, pages 770–778, 2016.
- [13] Yanping Huang, Youlong Cheng, Ankur Bapna, Orhan Firat, Mia Xu Chen, Dehao Chen, Hyouk Joong Lee, Jiquan Ngiam, Quoc V. Le, Yonghui Wu, and Zhifeng Chen. GPipe: Efficient training of giant neural networks using pipeline parallelism. Advances in Neural Information Processing Systems, 32, 2019.
- [14] Xianyan Jia, Le Jiang, Ang Wang, Wencong Xiao, Ziji Shi, Jie Zhang, Xinyuan Li, Langshi Chen, Yong Li, Zhen Zheng, Xiaoyong Liu, and Wei Lin. Whale: Efficient giant model training over heterogeneous gpus. In USENIX Annual Technical Conference. USENIX, 2022.
- [15] Zhihao Jia, Matei Zaharia, and Alex Aiken. Beyond Data and Model Parallelism for Deep Neural Networks. arXiv, 2018.
- [16] Shui Lam and Ravi Sethi. Worst case analysis of two scheduling algorithms. SIAM Journal on Computing, 6(3):518–536, 1977.
- [17] Chris Lattner, Mehdi Amini, Uday Bondhugula, Albert Cohen, Andy Davis, Jacques Pienaar, River Riddle, Tatiana Shpeisman, Nicolas Vasilache, and Oleksandr Zinenko. MLIR: Scaling compiler infrastructure for domain specific computation. In 2021 IEEE/ACM International Symposium on Code Generation and Optimization (CGO), pages 2–14, 2021.
- [18] Zhuohan Li, Siyuan Zhuang, Shiyuan Guo, Danyang Zhuo, Hao Zhang, Dawn Song, and Ion Stoica. TeraPipe: Token-Level Pipeline Parallelism for Training Large-Scale Language Models. 2021.
- [19] Deepak Narayanan, Aaron Harlap, Amar Phanishayee, Vivek Seshadri, Nikhil R. Devanur, Gregory R. Ganger, Phillip B. Gibbons, and Matei Zaharia. Pipedream: Generalized pipeline parallelism for DNN training. SOSP 2019 - Proceedings of the 27th ACM Symposium on Operating Systems Principles, pages 1–15, 2019.
- [20] Deepak Narayanan, Mohammad Shoeybi, Jared Casper, Patrick LeGresley, Mostofa Patwary, Vijay Korthikanti, Dmitri Vainbrand, Prethvi Kashinkunti, Julie Bernauer, Bryan Catanzaro, Amar Phanishayee, and Matei Zaharia. Efficient Large-Scale Language Model Training on GPU Clusters Using Megatron-LM. International Conference for High Performance Computing, Networking, Storage and Analysis, SC, 2021.
- [21] Alec Radford, Jong Wook Kim, Chris Hallacy, Aditya Ramesh, Gabriel Goh, Sandhini Agarwal, Girish Sastry, Amanda Askell, Pamela Mishkin, Jack Clark, et al. Learning transferable visual models from natural language supervision. In *International Conference on Machine Learning*, pages 8748–8763. PMLR, 2021.
- [22] Colin Raffel, Noam Shazeer, Adam Roberts, Katherine Lee, Sharan Narang, Michael Matena, Yanqi Zhou, Wei Li, and Peter J. Liu. Exploring the limits of transfer learning with a unified text-to-text transformer. Technical report, 2020.
- [23] Samyam Rajbhandari, Jeff Rasley, Olatunji Ruwase, and Yuxiong He. Zero: Memory optimizations toward training trillion parameter models. *International Conference for High Performance Computing*, *Networking, Storage and Analysis, SC*, 2020-Novem, 2020.
- [24] Jie Ren, Samyam Rajbhandari, Reza Yazdani Aminabadi, Olatunji Ruwase, Shuangyan Yang, Minjia Zhang, Dong Li, and Yuxiong He. ZeRO-offload: Democratizing billion-scale model training. 2021 USENIX Annual Technical Conference, pages 551–564, 2021.
- [25] Carlos Riquelme, Joan Puigcerver, Basil Mustafa, Maxim Neumann, Rodolphe Jenatton, André Susano Pinto, Daniel Keysers, and Neil Houlsby. Scaling vision with sparse mixture of experts. Advances in Neural Information Processing Systems, 34:8583–8595, 2021.
- [26] Noam Shazeer, Youlong Cheng, Niki Parmar, Dustin Tran, Ashish Vaswani, Penporn Koanantakool, Peter Hawkins, Hyouk Joong Lee, Mingsheng Hong, Cliff Young, Ryan Sepassi, and Blake Hechtman. Mesh-tensorflow: Deep learning for supercomputers. Advances in

Neural Information Processing Systems, 2018-Decem:10414–10423, 2018.

- [27] Mohammad Shoeybi, Mostofa Patwary, Raul Puri, Patrick LeGresley, Jared Casper, and Bryan Catanzaro. Megatron-LM: Training Multi-Billion Parameter Language Models Using Model Parallelism. 2019.
- [28] Colin Unger, Zhihao Jia, Wei Wu, Sina Lin, Mandeep Baines, Carlos Efrain, Quintero Narvaez, Vinay Ramakrishnaiah, Nirmal Prajapati, Pat Mccormick, Jamaludin Mohd-yusof, Jongsoo Park, Misha Smelyanskiy, Alex Aiken, Pat Mccormick, Jamaludin Mohd-yusof Xi, and Luo Dheevatsa. Unity: Accelerating DNN Training Through Joint Optimization of Algebraic Transformations and Parallelization This paper is included in the Proceedings of the. 2022.
- [29] Ashish Vaswani, Noam Shazeer, Niki Parmar, Jakob Uszkoreit, Llion Jones, Aidan N. Gomez, Łukasz Kaiser, and Illia Polosukhin. Attention is all you need. Advances in Neural Information Processing Systems, 2017-Decem:5999–6009, 2017.
- [30] Minjie Wang, Chien chin Huang, and Jinyang Li. Supporting very large models using automatic dataflow graph partitioning. *Proceedings* of the 14th EuroSys Conference 2019, 2019.
- [31] Yuanzhong Xu, HyoukJoong Lee, Dehao Chen, Blake Hechtman, Yanping Huang, Rahul Joshi, Maxim Krikun, Dmitry Lepikhin, Andy Ly, Marcello Maggioni, Ruoming Pang, Noam Shazeer, Shibo Wang, Tao Wang, Yonghui Wu, and Zhifeng Chen. GSPMD: General and Scalable Parallelization for ML Computation Graphs. 2021.
- [32] Fuzhao Xue, Ziji Shi, Futao Wei, Yuxuan Lou, Yong Liu, and Yang You. Go wider instead of deeper. In *Proceedings of the AAAI Conference on Artificial Intelligence*, volume 36, pages 8779–8787, 2022.
- [33] Lianmin Zheng, Zhuohan Li, Hao Zhang, Yonghao Zhuang, Zhifeng Chen, Yanping Huang, Yida Wang, Yuanzhong Xu, Danyang Zhuo, Joseph E. Gonzalez, and Ion Stoica. Alpa: Automating Inter- and Intra-Operator Parallelism for Distributed Deep Learning. 2022.