Atomic Defect-Aware Physical Design of Silicon Dangling Bond Logic on the H-Si(100)-2×1 Surface

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Abstract—**Although fabrication capabilities of *Silicon Dangling Bonds* have rapidly advanced from manual labor-driven laboratory work to automated manufacturing in just recent years, sub-nanometer substrate defects still pose a hindrance to production due to the need for atomic precision. In essence, unpassivated or missing surface atoms, contaminants, and structural deformations disturb the fabricated logic or prevent its realization altogether. Moreover, design automation techniques in this domain have not yet adopted any defect-aware behavior to circumvent the present obstacles. In this paper, we derive a surface defect model for design automation from experimentally verified defect types that we apply to identify sensitivities in an established gate library in an effort to generate more robust designs. Furthermore, we present an automatic placement and routing algorithm that considers scanning tunneling microscope data obtained from physical experiments to lay out dot-accurate circuitry that is resilient against the presence of atomic surface defects. This culminates in a holistic evaluation on surface data of varying defect rates that enables us to quantify the severity of such defects. We project that fabrication capabilities must achieve defect rates of around 0.1 %, if charged defects can be completely eliminated, or < 0.1 %, otherwise. This realization sets the pace for future efforts to scale up this promising circuit technology.**

I. Introduction & Motivation

With the decline of Moore's Law, research has turned to alternative circuit technologies in the search for promising post-CMOS candidates. A relatively new contestant in this domain are *Silicon Dangling Bonds* (SiDBs) that act as atomically-sized quantum dots and that have seen tremendous fabrication advancements in the recent years [1]–[7]. Under the term *atomic silicon quantum dots*, their application for the creation of nanometer-sized logic cells has been investigated which led to the successful demonstration of a sub-30 nm² SiDB OR gate and wire segments on hydrogen-passivated silicon surfaces [8]. Relying on Coulomb interaction instead of the transmission of electric current, SiDB logic implements the *Field-coupled Nanocomputing* (FCN) paradigm [9] that offers logic-in-memory devices [10], [11] and promises energy dissipation capabilities below the *Landauer limit* [10], [12]–[15], or clock frequencies in the terahertz regime [16]–[20].

Motivated by this, the research community has already taken interest in the SiDB platform for logic design; an effort that resulted in the creation of various physical simulators [18], [19], [21]–[24], various manually designed circuits and some gate libraries [18], [20], [21], [25]–[29], as well as algorithms for placement and routing of SiDB gates [28], [30].

However, SiDB fabrication requires atomic precision and, thus, is prone to substrate defects at the sub-nanometer level. These defects naturally occur during the substrate preparation, i.e., in the process of preparing a pure hydrogen-passivated silicon (H-Si(100)-2×1) surface for SiDB fabrication. They are generally classified as any atomic structure that does not follow the H-Si(100)-2×1 surface reconstruction, in which each surface silicon atom is bonded to a neighboring silicon atom creating a dimer pair, a hydrogen atom from the passivation, and two silicon atoms in the bulk of the crystal [31]. Such defects could include unpassivated surface silicon atoms, missing silicon atoms, contaminant atoms, or structural deformations (which is covered in more detail in Section III).

Current fabrication of SiDB logic necessitates the scanning for defect-free regions that are large enough to host the intended layout on the substrate at hand [32]. While being a useful proof-of-concept demonstration, this fabrication approach is not only wasteful, but also increasingly unrealistic with growing layout size as it can accommodate for a handful of gates at the utmost. Hence, the presence of surface defects imposes a hindrance on scaling SiDB design size. At the same time, operating at the atomic-scale, material defects are largely common at the current fabrication capabilities.

Accordingly, the electrostatic effects of such surface defects have been closely examined—providing insights into how they might limit SiDB fabrication and the operation of fabricated SiDB devices [33], [34]. This work leverages these defect analysis findings to enable automatic layout design under the presence of atomic surface defects.

In this regard, the paper at hand proposes the following contributions:

1) the derivation of an atomic defect model by the establishment of equivalence classes among 13 experimentally verified H-Si(100)-2×1 defect types to guide design automation methodologies,

2) a case study of applying said defect model to the established *Bestagon* gate library [28], which led to the identification of sensitivities of some gates to certain defects for which we propose more robust redesigns,

3) an automatic placement and routing algorithm that considers real *Scanning Tunneling Microscope* (STM) surface scans obtained from physical experiments as well as simulated surface data to design functioning dot-accurate SiDB circuit layouts in the presence of atomic surface defects by avoiding disturbed regions, and

4) a culmination of the previously mentioned contributions into a holistic experimental evaluation on H-Si(100)-2×1 surfaces of variable defect rates that quantifies the severeness of—particularly—charged atomic defects.
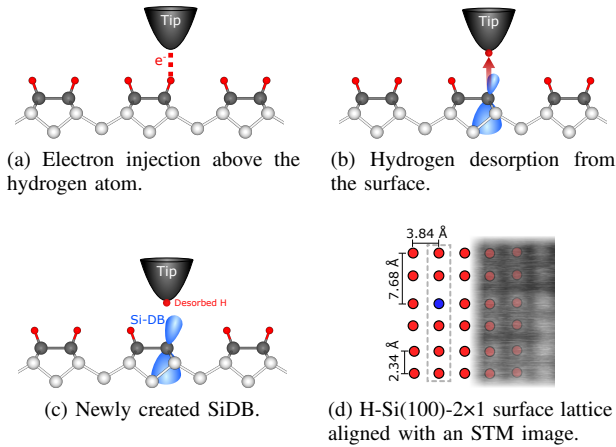
(a) Electron injection above the hydrogen atom.

(b) Hydrogen desorption from the surface.

(c) Newly created SiDB.

(d) H-Si(100)-2×1 surface lattice aligned with an STM image.

Fig. 1: Illustration of the SiDB fabrication process on the H-Si(100)-2×1 surface using an STM tip. The atomic surface structure is depicted as a side-view ball-and-stick model.

Thereby, we propose the first defect-aware framework for SiDB logic that amalgamates fabrication and design automation. Experimental evaluations on both real and simulated H-Si(100)-2×1 surfaces allow us to estimate the required surface manufacturing quality in terms of the defect rate for large-scale SiDB device fabrication in future efforts to be around $0.1\,\%$, if charged defects can be completely eliminated or $< 0.1\,\%$, otherwise.

The remainder of this manuscript is structured as follows: in an effort to establish this paper as a stand-alone work, Section II reviews related material on SiDB fabrication and their logic platform to constitute the foundation upon which this paper is built. Afterward, Section III introduces atomic defects on the H-Si(100)-2×1 surface and discusses their effects on SiDB systems. Based on that, Section IV presents the proposed defect-aware physical design methodology by first establishing a surface defect model and, then, discussing algorithmic details. An experimental evaluation of the approach is conducted in Section V. Finally, Section VI concludes the paper and gives an outlook on future work in the domain.

II. SILICON DANGLING BOND LOGIC

As an implementation of the FCN paradigm [9], the utilization of SiDBs has recently gained momentum. Using an atomically-sharp tip of a *Scanning Tunneling Microscope* (STM), individual dangling bonds can be created on a hydrogen-passivated silicon surface at the single-atom scale [2]–[4], [35]–[39]. These dangling bonds act as quantum dots and are used to represent logic states and to realize Boolean operations at the limit of physical scaling [1], [5], [8], [40], [41].

The most commonly used surface phase for SiDB creation is H-Si(100)-2×1 whose atomic structure is illustrated in Fig. 1. The surface consists of discretely defined sites (shown as red atoms in Fig. 1d), where SiDBs can be fabricated with atomic precision. By using the scanning probe tip to inject current into the H-Si bond, it is possible to selectively remove single hydrogen atoms from the surface, leaving behind an SiDB (shown in blue in Fig. 1b–1d).

The resulting SiDBs may possess 0, 1, or 2 electrons, corresponding to positive, neutral, and negative charge states, respectively.[1]

[1]Note that, in the following only negative or neutral dangling bonds are of interest. Positively charged ones are not relevant for gate configurations [8], [21]
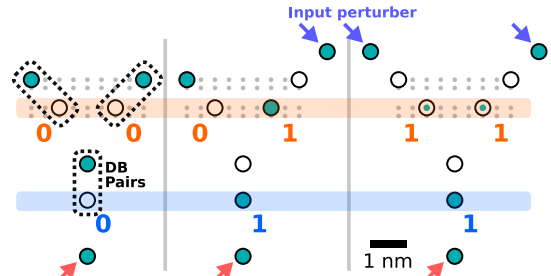

Fig. 2: Conceptual recreation of the SiDB OR gate proposed and fabricated on the H-Si(100)-2×1 surface by Huff *et al.* [8].

The corresponding charge states can be controlled by environmental factors such as the bulk dopant concentration [42] and the presence of electric fields [36], [40]. A groundbreaking demonstration by Huff *et al.* has experimentally demonstrated that careful configurations of pairs of SiDBs can be used to realize logic components [8]. These SiDB pairs are observed to share a single additional electron between them which can be manipulated to occupy the left or right SiDB of the pair indicating a binary 0 or 1 state; a behavior that was coined *Binary-Dot Logic* (BDL) [8].

These electronic properties enable the realization of BDL wire structures as well as a sub $30\,\mathrm{nm}^2$ logic OR gate [8]. A simulated reproduction of the OR gate using the SiDB simulator *SiQAD* [21] is shown in Fig. 2. Here, the input bit states are set by the addition of a peripheral SiDB, dubbed a *perturber* [8], [21], which exerts an external field on the input SiDB pair to emulate the presence of an input BDL wire at the logic 1 state. When one or both of the input SiDB pairs are set to logic 1 by input perturbers, the output also toggles to logic 1 as expected of an OR gate. It is to be noted that the need for these perturbers will be alleviated upon the future development of I/O devices.

The recent physical accomplishments and the upcoming commercialization [43], [44] in the domain of SiDB logic have triggered an increasing interests in design automation methods for this technology—yielding first CAD tools, circuit layouts, and physical design algorithms [18]–[30]. However, none of these methodologies and proposals take into account that the fabrication of sub-nanometer structures is naturally error-prone and that atomic defects of the substrate are inherent to this endeavor and will continue to be for the foreseeable future [33], [34]. The following section covers common atomic defects on the H-Si(100)-2×1 surface and their influence on SiDB logic.

III. ATOMIC SURFACE DEFECTS

Despite the relative cleanliness of H-Si(100)-2×1 compared to other crystal faces of silicon [31], there still exists a natural concentration of defects that cannot be completely avoided with current *in-situ* preparation methods. These defects can be broadly described as any collection of atoms in the crystal that do not form the 2×1 surface phase, where each surface silicon atom is host to only one hydrogen. These could include unpassivated surface silicon atoms, missing silicon atoms, contaminant atoms, or structural deformations. To this end, defects prevent the creation of atomically identical SiDBs due to their varying structures. Additionally, the proximity of defects alters SiDB behavior and, consequently, corrupts implemented logic gates.

As an example, Fig. 3a depicts an empty states STM scan acquired at $1.3\,\mathrm{V}$ and $50\,\mathrm{pA}$ of a physically fabricated H-Si(100)-2×1 surface.
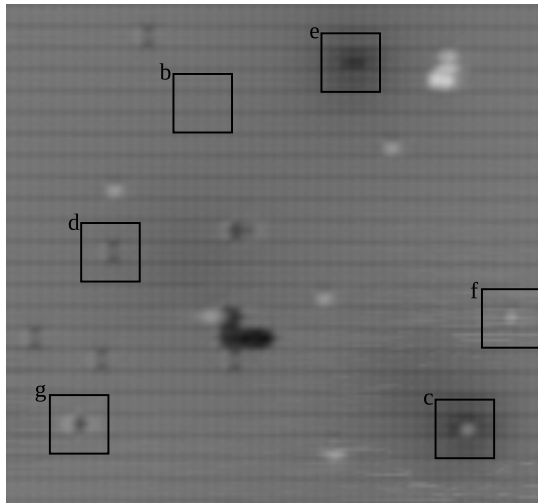
(a) STM surface scan of $19\,\text{nm} \times 18\,\text{nm}$ with visible defects.
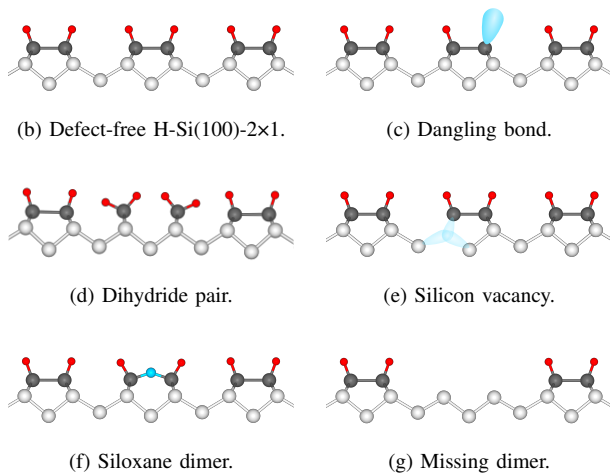
(b) Defect-free H-Si(100)-2×1.

(c) Dangling bond.

(d) Dihydride pair.

(e) Silicon vacancy.

(f) Siloxane dimer.

(g) Missing dimer.

Fig. 3: A H-Si(100)-2×1 surface and common atomic defects found thereon depicted as side-view ball-and-stick models.

The black frames with alphabetical labels indicate different atomic defects. Fig. 3b to Fig. 3g illustrate these defects as a side-view ball-and-stick model. The following list gives a brief explanation of their nature:[2]

3b The defect-free H-Si(100)-2×1 surface phase. Each surface silicon atom in dark gray is paired with another surface silicon atom creating a dimer pair. Each silicon atom of a dimer is then passivated with a single hydrogen atom. Each silicon atom in this configuration is capable of hosting a single, chemically identical dangling bond.

3c A silicon atom that is not terminated with hydrogen leaving a dangling bond. These can be intentionally created, or found from incomplete hydrogen passivation.

3d A dihydride pair, where no dimer bond forms, leaving each silicon atom to bond with two hydrogen atoms. Dihydrides are found more often when the crystal annealing temperature is too low [45].

3e A silicon vacancy, where a single silicon atom is missing from the lattice leaving unsatisfied subsurface dangling bonds.

[2]A more detailed discussion of these and other commonly occurring defects can be found in [33].
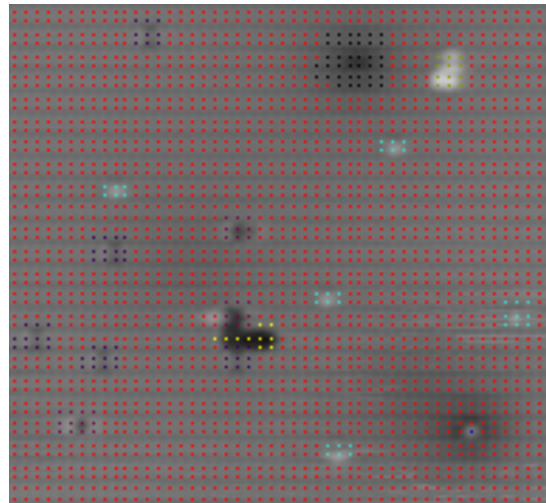

Fig. 4: The same STM image as shown in Fig. 3a with a lattice overlay. Color key: *red*: defect-free H-Si, *blue*: dangling bond, *black*: silicon vacancy, *purple*: dihydride pair, *magenta*: missing dimer, *light blue*: siloxane and similar, *yellow*: etch pit (multiple missing dimers), *gold*: unknown.

3f A siloxane dimer, which features a single oxygen atom between the two silicon atoms of the dimer. This defect occurs in high concentration when the preparation chamber is contaminated with water molecules.

3g A missing dimer where both silicon atoms are absent.

Atomic defects can furthermore also appear in various combinations on the same or adjacent dimers which increases their affects on logic placed in their vicinity [33].

To the best of the authors' knowledge, no related work on SiDB logic and design automation has considered the impact atomic defects have on their proposed layouts. This disregard of physical effects leaves most approaches conflicting with existing fabrication capabilities.

In the following section, we are addressing this shortcoming by proposing a physical design methodology that is aware of atomic defects. Consequently, the layouts automatically generated by the proposed approach avoid defective surface positions.

IV. DEFECT-AWARE PHYSICAL DESIGN

In this section, we introduce a solution that addresses the shortcomings of existing physical design methods for SiDB logic discussed above. To this end, we first propose an abstract surface defect model for automatic design that is based on the physical properties of the identified atomic surface defects. Afterward, we propose a defect-aware physical design method that, utilizing the proposed model, is able to realize SiDB logic that behaves as intended on an otherwise defective surface.

A. Surface Defect Model

Before being able to apply any defect-aware design methodology, the atomic structure of the specific surface at hand must be analyzed and defects identified. In this instance, defects are autonomously classified using a *Convolutional Neural Network* (CNN) similar to that developed in [32]. Its input is an STM image like that in Fig. 3a. The CNN provides a pixel-based classification of the surface corresponding to the defect types as its output. The classification is then correlated to the lattice positions of the H-Si(100)-2×1 surface

yielding a coordinate-based defect assignment as shown in Fig. 4. Hydrogen-terminated silicon (defect-free dimers) is labeled in red, while various defects are labeled as described in the caption.[3]

Once each lattice position has been classified, the atomic defects of the H-Si(100)-2×1 surface can be further divided into two categories: *charged* and *uncharged* (neutral). The overall charge of a defect is dependent on both the atomic structure and the crystal doping level. Since the crystals considered in this work are degenerately n-doped, all electron energy levels within the band gap are filled resulting in negatively charged defects.

These residual negative charges (as observed in dangling bond and silicon vacancy defects) are able to exert screened Coulombic effects on the charge state of nearby SiDBs as demonstrated by experiments in the literature [34]. Different gates may have a varying tolerance against these effects, which can be found by running fixed charge defect simulations for defect types of interest using *SiQAD* [21], [46]. The physical parameters of silicon vacancy defects have been fitted in [34] and recreated in simulation in [46]. With these resources, we have developed the following procedure to determine the minimum distance that each gate tile of a given library must avoid a defect by in order to achieve correct logic operation for that tile in isolation:

1) Place the defect at distance d from the gate.
2) Run physical simulations of the gate toggling through all possible input signal combinations.
3) For each simulation run, check that the input and output SiDB pairs hold the correct binary logic state.
4) If any input combination results in incorrect logic states, return d as the minimum avoidance distance.
5) Repeat for a sufficient count of defect locations and values of d to cover meaningful distances in the vicinity of the gate.

We have applied this procedure to the *Bestagon* gate library [28] with silicon vacancy defects placed at $7.68\,\text{Å}$ spacings in both x and y directions, $4\,\text{Å}$ under the surface within a $\approx 30\,\text{nm} \times 30\,\text{nm}$ grid centered on each gate. We have found that some Bestagon tiles are not functional at any tested defect distance, necessitating the redesign of these nonfunctional logic tiles. We have, therefore, redesigned them using an automated SiDB layout designer based on reinforcement learning [47] and selected candidates that have the lowest minimum avoidance distances. The global minimum avoidance distance was found to be $10\,\text{nm}$ by taking the worst performing minimum avoidance distance out of all tiles. A repository is made publicly available on GitHub[4] containing 1) *SiQAD* design files of the redesigned tiles, 2) evaluation results for minimum avoidance distance of these tiles, 3) the original Bestagon tiles, and 4) a list of nonfunctional tiles that do not have a proposed direct replacement.

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[3]Looking at the defect lattice positions, one can see that some assigned labels extend farther than the underlying physical defect. This is due to the output of the CNN. When labeling the training data, defects were marked based on their contrast in the acquired images and not the exact lattice coordinates. Since some defects had a strong influence on the contrast of adjacent, defect-free atoms, they were labeled as the same defect to avoid any aliasing in defect classification. It is possible to apply a filter as a post-processing step to limit each defect label to its exact atomic position as shown for the dangling bond defect (in blue) near the bottom-right corner of Fig. 4. Since it is necessary to keep some distance from the various defects anyway, such filtering is not a crucial step of the proposed methodology. However, localizing stray dangling bond defects with atomic accuracy can be beneficial in another way: if they happen to coincide with SiDB positions of placed gates, they can be seamlessly integrated rather than considering them as defects that must be avoided.

[4]https://github.com/cda-tum/sidb-defect-aware-physical-design
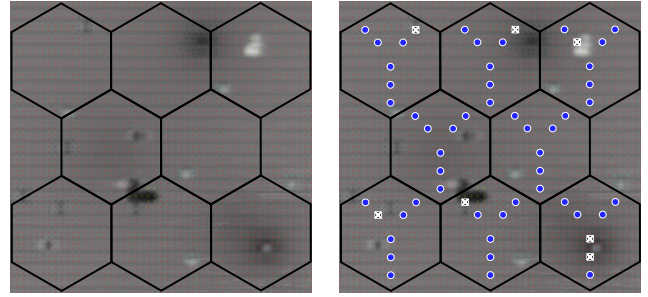
(a) Overlaying a hexagonal surface tiling. Each tile can hold up to one SiDB gate or wire segment.

(b) Matching Huff *et al.*'s SiDB OR gate (cf. Fig. 2) [8] against every tile. Crossed-out black dots indicate a conflict with a present atomic defect at that position.

Fig. 5: The STM surface scan with atomic defects from Fig. 3 and Fig. 4 with a hexagonal tiling and a gate overlay.

The latter applies foremost to the half-adder tile which can however be decomposed into, e.g., an XOR and an AND tile.

B. Automatic Physical Design

The de-facto standard for physical design in the FCN domain is that of a tile-based abstraction [48]–[53]. That is, a (uniform) tiling of a surface is provided where each tile can implement one designated Boolean function. A standard library of pre-designed SiDB gates and wire segments can be applied to generate a dot-accurate layout from such a gate-level abstraction. Thereby, the focus is shifted from the physical to the logic level and, thus, assists placement and routing by limiting the search space [51]–[54]. Additionally, logic-level simulation and verification are enabled [55].

Surface tilings come in manifold forms with the most common one being the Cartesian grid where each tile is a rectangle [48], [49], [56], [57]. Recently, hexagonal tilings were established for SiDBs [28], because they intrinsically match the Y-shaped SiDB gates that have been experimentally proven by Huff *et al.* [8], and as such provide a more realistic abstraction for SiDB circuit layouts.

This work, thus, also relies on tile-based design. In the following, we assume a hexagonal tiling together with established SiDB gates [28]. However, our approach is generic such that any tiling and any standard library can be applied.

Instead of imagining a perfect, idealized surface, we consider a realistic STM surface scan as input to our algorithm. We overlay a tiling and match each gate and wire of a given gate library in every rotation against each tile and analyze the effects of defects in the proximity of each dot that make up the gate/wire tile. This procedure yields a blacklist of gate-tile pairs, i.e., a listing of SiDB structures that cannot operate properly on certain tiles of the surface.

We pass this blacklist as a set of placement and routing constraints to a satisfiability-based algorithm that avoids placing those gates/wires on the specified tiles in the specified rotation. The result is a dot-accurate layout that avoids all defects on the surface and, thus, preserves functionality in the presence of disturbances.

The following example shall illustrate this process. Assume the STM surface scan depicted in Fig. 3 was to be used as input to the proposed defect-aware physical design algorithm together with Huff *et al.*'s SiDB OR gate [8] as the target technology. The detected defects are to be avoided while employing a tile-based design paradigm for abstraction and search space restriction. Fig. 5a shows

TABLE I: Layout data obtained from physical design on experimentally fabricated and simulated H-Si(100)-2×1 surfaces.

	Benchmark [28]		Examined Surface Data															
			Experimental STM Scans				Simulated w/ Charged Defects						Simulated w/o Charged Defects					
	defect-free		8.57% defective		6.26% defective		1% defective		0.5% defective		0.1% defective		1% defective		0.5% defective		0.1% defective	
Name	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]	#SiDBs	A[nm²]
xor2	59	979.55	—	—	—	—	58	1120.67	59	979.55	58	1120.67	59	1268.12	59	979.55	59	979.55
xnor2	63	979.55	—	—	—	—	62	1120.67	63	979.55	62	1120.67	63	1268.12	63	979.55	63	979.55
par_gen	99	1956.15	—	—	—	—	—	—	97	2094.47	111	1882.72	98	1898.50	98	1956.15	98	1956.15
mux21	177	3447.67	—	—	—	—	—	—	—	—	230	5540.22	—	—	163	3842.41	179	5533.14
par_check	317	6051.59	—	—	—	—	—	—	—	—	358	7924.58	—	—	382	20899.23	229	6577.13
xor5_r1	200	3447.67	—	—	—	—	—	—	216	7524.68	174	4682.02	—	—	198	5629.58	210	3941.50
xor5_majority	191	3445.16	—	—	—	—	—	—	209	7524.68	166	4682.02	181	5533.14	205	5629.58	257	5926.85
t	459	7924.58	—	—	—	—	—	—	—	—	443	8724.82	—	—	541	20502.28	424	9768.67
t_5	482	7924.58	—	—	—	—	—	—	—	—	458	8941.14	—	—	487	17122.00	436	10416.59
c17	341	6330.29	—	—	—	—	—	—	—	—	391	7924.58	—	—	598	20577.78	466	10316.02
majority	545	10445.78	—	—	—	—	—	—	—	—	538	15306.82	—	—	—	—	665	14301.76
majority_5_r1	509	9518.88	—	—	—	—	—	—	—	—	570	11743.40	—	—	—	—	925	17490.35
cm82a_5	928	17502.73	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1579	31776.18
newtag	511	9518.88	—	—	—	—	—	—	—	—	568	15306.82	—	—	—	—	665	15098.90

a hexagonal tiling laid over said STM surface scan from Fig. 3. Note that the size and rotation of the hexagons depend on the applied standard library.

In Fig. 5b, Huff *et al.*'s OR gate is matched against each tile and the effects of present defects on each SiDB are analyzed. The SiDBs indicated with a crosed-out black dot conflict with surface defects. Any gate that has at least one conflicting SiDB is excluded from being placed on that particular tile in that particular rotation. The same is repeated for all rotations of all gates/wires in the given standard library. This procedure yields the aforementioned placement blacklist.

For any given circuit specification, the resulting placement and routing problem with the blacklist is encoded as a satisfiability instance as successfully demonstrated in [51], [52]. A satisfying solution to the instance yields a conflict-free placement and routing on the surface. Due to the search space restrictions that have been employed by relying on tile-based design, it cannot be guaranteed that no such solution exists if the satisfiability instance returns `UNSAT`. However, the specification can be resynthesized and/or the tile overlay shifted across the surface in order to attempt finding a satisfying solution.

V. Experimental Evaluations

In this section, we present and discuss the results of an experimental evaluation of the proposed defect-aware physical design approach. To this end, we applied the algorithm to automatically generate SiDB layouts on defective H-Si(100)-2×1 surfaces, both real and simulated. The following Section V-A goes over our experimental setups while Section V-B discusses the results and their implications.

A. Experimental Setups

1) Fabrication: Of the surfaces used in this evaluation, two were experimentally fabricated in a lab and measured with an STM, the others were simulated based on experimental findings.

The STM measurements were performed using an Omicron LT-STM system operating at $4.5\,\mathrm{K}$ and ultra-high vacuum ($3 \times 10^{-11}\,\mathrm{Torr}$). The STM tips were electrochemically etched from tungsten wire and sharpened using a field ion microscope [58]. The used samples are highly arsenic-doped ($\approx 1.5 \times 10^{19}\,\frac{\mathrm{atoms}}{\mathrm{cm}^3}$). They were prepared *in-situ* via resistive heating. To this end, they were first degassed at $600\,^\circ\mathrm{C}$ overnight followed by multiple flash annealing cycles at $1250\,^\circ\mathrm{C}$. Finally, the samples were hydrogen-terminated at $330\,^\circ\mathrm{C}$ while exposing their surface to molecular hydrogen ($10^6\,\mathrm{Torr}$). The H_2 gas was converted to atomic hydrogen using a tungsten filament held at $1600\,^\circ\mathrm{C}$.

The image acquisition was done using a Nanonis SPM controller with respective software. All images were taken in constant height mode with an imaging bias of $1.3\,\mathrm{V}$ and a current setpoint of $50\,\mathrm{pA}$.

2) Programming: The architecture and training of the neural network used for defect identification in STM scans is modeled after [32] and implemented in Python using Keras with the TensorFlow backend. As an addition, the training data was expanded by a factor of three and the number of classes increased to a total of 13 different defect types. The proposed defect-aware physical design algorithm was implemented in C++17 on top of the *fiction* framework [59] as part of the *Munich Nanotech Toolkit* (MNT).[5] The utilized SMT solver is *Z3* [60]. All experiments were compared against the state-of-the-art results for defect-free SiDB layouts presented in [28]. The obtained layouts were formally verified for logical correctness using the approach presented in [55]. All evaluations were run on a Manjaro 23 machine with an AMD Ryzen 7 PRO 5850U CPU with $1.90\,\mathrm{GHz}$ (up to $4.40\,\mathrm{GHz}$ boost) and $32\,\mathrm{GB}$ of DDR4 main memory.

B. Results

The STM scans of the fabricated H-Si(100)-2×1 surfaces span a total of 830×652 and 740×1090 hydrogen sites, respectively, of which 8.57% and 6.26% are defective.[6] We applied the proposed atomic defect-aware physical design algorithm to generate the same set of benchmark circuits used in [28] while obeying the presented surface defect model, and using the *Bestagon* gates that we redesigned for defect robustness.

The results for these cases are listed in Table I under the caption Experimental STM Scans. For all evaluations, we list the number of required SiDBs to implement each circuit and its bounding box area in nm^2. As can be seen, not a single layout could be successfully generated—as is indicated by the dashes—due to the relatively high defect rates of the fabricated samples—highlighting the critical severity of atomic defects in logic design.

To this end, we strive for quantifying their impact by evaluating simulated surfaces of comparable size with variable defect rates of 1%, 0.5%, and 0.1%, once with both charged and neutral atomic defects, and once with only neutral defects, using the same benchmark set. The obtained results can be found in the same table under the caption Simulated w/ Charged Defects for surfaces including charged defects, and under Simulated w/o Charged Defects for surfaces with purely neutral defects. In both cases, defect types were automatically distributed in accordance with experimental findings. In the former case, charged ones make up 5% of all defects.

Three core findings can be obtained from these results: 1) defect avoidance directly correlates with significantly larger overall area consumption, 2) high defect rates, and particularly charged defects, have a tremendous impact on layout generation to the degree where

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[5]Publicly available at `https://github.com/cda-tum/fiction`.
[6]Not counting stray DB defects, as they can be erased from the surface prior to the fabrication of circuitry [2].

circuits cannot be realized in their vicinity at all, and 3) fabrication capabilities must achieve a defect rate of around 0.1 % in the absence of charged defects or < 0.1 % with charged defects present to enable sophisticated layout manufacturing.

VI. Conclusions

Fabrication capabilities of *Silicon Dangling Bonds* (SiDBs) have advanced to the automated manufacturing stage. Nevertheless, atomic substrate defects are currently preventing technology scaling as they disturb gate functionalities or prevent logic realization altogether. In this work, we presented a surface defect model to guide physical design that we obtained by investigating 13 experimentally verified H-Si(100)-2×1 defect types. Furthermore, we proposed modifications to an established SiDB gate library to increase its robustness against substrate defects. Finally, we proposed a defect-aware placement and routing algorithm that considers STM surface scans obtained from experimentation as well as simulated surface data and designs functioning SiDB circuit layouts in the presence of atomic defects. An experimental evaluation on real fabricated surfaces demonstrated its functioning but also highlighted the limitations of current fabrication capabilities. We demonstrated the critical impact that charged defects have on the creation of circuit layouts and determined a defect rate of around 0.1 %, if charged defects can be completely eliminated, or < 0.1 %, otherwise, to be required for the future of large-scale SiDB logic manufacturing. Herewith, this work represents an amalgamation of fabrication and design automation that provides the basis for large-scale defect-aware physical design of SiDB circuitry.

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