Temperature Behavior of Silicon Dangling Bond Logic

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***Abstract*— *Silicon Dangling Bonds* (SiDBs) on the hydrogen-passivated silicon surface have emerged as a promising competitor in the realm of beyond-CMOS computational technologies. They have attracted the attention of academia and industry due to their greatly increased integration density and energy efficiency compared to contemporary fabrication nodes. Since information propagation and computation in the SiDB domain are based on electrostatic field coupling, SiDBs are considered as a room temperature-enabled technology. However, the effect of temperature on SiDB-based gates and their operation has not yet been considered. Consequently, established design automation flows and gate library proposals are temperature-agnostic without any guarantee of their operability in real-world scenarios. In this paper, we investigate for the first time the effect of temperature on the operation of SiDB-based gates. To this end, we utilize a newly developed temperature-aware simulator and exhaustively evaluate previously fabricated gates and theoretically proposed standard libraries. The results reveal significant temperature-sensitivity of many gates, highlighting the crucial role of considering temperature behavior in the realization of SiDB-based gates. Therefore, it is imperative to minimize the use of such temperature-sensitive components in future designs and to develop more robust standard gates. This research serves as the foundation for subsequent studies and is vital for the acceleration of the development of this promising green nanotechnology.**

I. Introduction & Motivation

In the recent years, there has been growing interest in the *Silicon Dangling Bond* (SiDB) logic platform—a new computational nanotechnology that can potentially outperform current CMOS technology nodes in terms of several key metrics [1]–[7]. One of the main features of SiDBs is the sub-nanometer elementary devices that allow for a significant increase in the integration density compared to current CMOS fabrication methods [4], [6]–[11]. Additionally, the SiDB logic operates through Coulombic repulsion of charges rather than the flow of electric current [4], [8], resulting in ultra-low energy dissipation and making it a potential green alternative in the beyond-CMOS domain [8], [11]–[14]. Furthermore, it has been suggested as a potential candidate for the integration of quantum computers [15] and compatibility with conventional CMOS circuitry [7].

Due to the potential benefits of SiDB logic, researchers have proposed various gate and circuit libraries [16]–[22] as well as design automation solutions [16], [18], [23], [24], to realize logic in this technology. Furthermore, there is also increasing commercial interest in SiDBs, as demonstrated by companies such as *Quantum Silicon Inc.* which aims to be an early adopter of this technology and has secured significant investments for this purpose [25], [26].

However, despite the significant interest in the SiDB logic platform, the accurate simulation of its electrostatic behavior remains a challenging task. While previous solutions have been proposed [16], [20], [27], they have not taken into account the effects that thermal energy has on charge distributions. This lack of consideration of environmental influences may lead to inaccurate prediction of circuit behavior. This is particularly striking, since although SiDBs are proclaimed as a room temperature enabled technology [3], also experimental fabrication at cryogenic temperatures [8], [11] exists. Therefore, when the technology is used on such a broad spectrum of temperatures, it is imperative to take thermal energy into account.

In this paper, we investigate for the first time the effect of temperature on the operation of SiDB-based gates. To this end, we utilize a newly developed temperature-aware physical simulator and exhaustively evaluate previously fabricated SiDB-based gates and theoretically proposed standard libraries. This will ultimately lead to a better understanding of SiDB-based gates and inform the design and optimization of such systems.

The results of our evaluation demonstrate the exceptional capability of SiDB gates to perform reliably at temperatures well above the conventional room temperature range. This remarkable feature highlights the potential of this cutting-edge nanotechnology, underscoring its promise as a revolutionary and transformative force in the field. In contrast, it is revealed that SiDB-based gate libraries proposed in the literature possess a high sensitivity to thermal noise, emphasizing the importance of incorporating temperature behavior into design automation flows and the synthesis of new gate libraries.

The organization of this manuscript is designed to provide a comprehensive overview of the temperature influence on SiDB-based gates. In Section II, background information required for the comprehension of the SiDB technology is provided. In Section III, we present the fundamental physical concepts that are incorporated into the newly proposed simulation approach. Additionally, the *Critical Temperature* is introduced, which is the output of the simulator and is a measure to describe at which temperature the reliable execution of SiDB gates becomes affected defined by a given desired computational accuracy. Afterward, extensive experimental results and their discussion are presented in Section IV, which demonstrate the influence of temperature on SiDB-based gates. Finally, in Section V, we conclude the work by summarizing the key findings and highlighting the potential for future research in this field.

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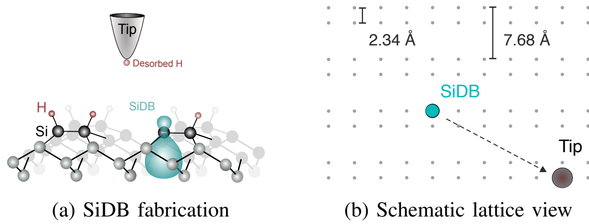


(a) SiDB fabrication (b) Schematic lattice view

Fig. 1: Fabrication of SiDB layouts.

II. Preliminaries

This section lays the informational foundation required for understanding this article. In Section II-A, we discuss the SiDB logic platform and its fabrication, while Section II-B describes established physical simulation methodologies. Due to page limitations, we kept the respective descriptions brief; for a more detailed rendition of the relevant subjects please refer to [16].

A. The SiDB Logic Platform

SiDBs are created by using a *Scanning Tunneling Microscope* (STM) to apply a voltage to a *Hydrogen-passivated Silicon* (H-Si) surface. The voltage breaks the bond between a silicon and a hydrogen atom. The hydrogen atom is desorbed, leaving an open valence bond [4]–[6], [28]–[32]. These steps are sketched in Fig. 1a with the tip desorbing the hydrogen atom and the formation of an SiDB. After the first SiDB is generated, the tip moves to a new Si-dimer to desorb the next hydrogen atom. This basic principle of the fabrication process is sketched in Fig. 1b. Each SiDB created in this way acts as a chemically-identical quantum dot that can confine a maximum of two electrons and is in one of three different states: negatively, neutrally, or positively charged. The energy levels of the charge transition in SiDBs are within the band gap—making their states stable unless perturbed by other charges [10], [33]. In n-doped systems with a surface depletion region near the surface, SiDBs retain their quantum dot character but tend to be negatively charged due to an increased Fermi energy. This property is exploited to create logic elements such as gates using SiDBs. SiDBs can be paired in metastable configurations where the state of one SiDB affects the other through band bending—creating a concept known as *Binary Dot Logic* (BDL). The first experimental implementations were performed by Huff *et al.* [8] who were able to demonstrate a working sub-$30\,\mathrm{nm}^2$ OR gate and multiple wire segments using SiDBs.

B. Simulation of Valid Charge Distributions

Investigating this nascent technology and validating the designs of newly proposed circuits requires a thorough physical simulation of SiDB layouts. This can be accomplished by drawing upon the principles of electrostatics, which dictate that the electrostatic potential energy between two entities decreases as the inverse of the distance between them ($1/d$) in both free space and dielectric materials.

However, when considering SiDBs, the electric charges in their vicinity necessitate the consideration of an additional exponential fraction on top of the inverse distance. This leads to the expression of an electric potential $V_{i,j}$ at position i generated by an SiDB in state $n_j \in \{-1,0,1\}$ located at position j [8], [29] as:

$$V_{i,j} = -\frac{q_e}{4\pi\epsilon_0\epsilon_r} \cdot \frac{e^{-\frac{d_{i,j}}{\lambda_{tf}}}}{d_{i,j}} \cdot n_j \tag{1}$$

In this formula, λ_{tf} defines the *Thomas-Fermi screening length* and ϵ_r the *dielectric constant* which were experimentally extracted to be $5\,\mathrm{nm}$ and 5.6, respectively [8]. Furthermore, ϵ_0, q_e and $d_{i,j}$ are the *vacuum permittivity*, the *electron charge ($q_e = -e$; e: elementary charge)*, and the *Euclidean distance* between position i and j, respectively.

Due to the *electrostatic superposition principle*, a layout's total electrostatic potential energy E is then given by [34]:

$$E = -\sum_{i<j} V_{i,j} \cdot n_i \cdot q_e \tag{2}$$

However, not all possible charge distributions are feasible, as they must adhere to the principle of *metastability*, which encompasses two key criteria: *population stability* and *configuration stability*. Both must be satisfied to ensure the validity of the simulation results. The number of physically valid charge distributions for a particular SiDB layout can vary significantly. Smaller layouts consisting of a few SiDBs tend to have only one physically valid charge distribution, whereas larger SiDB gates can have significantly more valid states than they possess SiDBs.

Several algorithms have been introduced to minimize Eq. (2) while satisfying metastability. Two algorithms represent the current state of the art: *ExhaustiveGS* (ExGS) [17], [20] and *SimAnneal* [16]. ExGS covers the entire search space, and therefore, always determines all physically valid charge states (at the expense of scalability). In contrast, SimAnneal is a heuristic (and hence, much more scalable) approach but accordingly, only produces approximate results.

However, all these existing algorithms do not take the temperature into account, which may lead to deviations between the real-world behavior and simulation results. In this work, we investigate the effect of temperature on the operation of SiDB-based gates. To this end, a newly developed simulator is utilized, which is briefly reviewed next.

III. Temperature-aware Simulation

Investigations on the effect of temperatures on the SiDB-based gates have been conducted utilizing a newly developed temperature-aware simulator which has been implemented on top of the *fiction* toolset. In this section, we first introduce the simulator's underlying principle (based on the *Canonical Partition Function* from statistical physics). Afterwards, we explain how this concept is applied to simulate the *Critical Temperature*. It is the output of the simulator and is defined to describe at which temperature the reliable execution of SiDB-based gates cannot be guaranteed, because the probability of computing the correct output falls below a given confidence level.

A. Partition Function

In this section, we introduce the *Partition Function*, which is the basic physical concept that allows to simulate the behavior of SiDB-based gates as a function of the temperature. It is defined as the sum of the Boltzmann factors $e^{-E_i/k_B T}$, with k_B being the Boltzmann constant, for all possible states of the system with the energy E_i, the state degeneracy factor g_i, and the system temperature T [35], [36].

A special partition function is the so-called *Canonical Partition Function* (CPF) Z_C, which is used to describe physical systems in thermal equilibrium at a fixed temperature T and is given as:

$$Z_C = \sum_i g_i \cdot e^{-E_i/k_B T} = \sum_i g_i \cdot e^{-\beta E_i} \tag{3}$$

Applying the CPF, we can calculate the probability p_i that an SiDB system occupies a given charge distribution state i, which is determined by:

$$p_i = \frac{g_i}{Z_C} e^{-\beta E_i} \tag{4}$$

Calculating p_i for a given SiDB system (for all physically valid charge states i) directly corresponds to a temperature sensitivity analysis. This is because Eq. (4) (which contains Eq. (3)) yields the individual occupancy probabilities of the system at temperature T. Consequently, as outlined above, the probabilities allow a direct inference of the system's stability.

B. Critical Temperature Determination Through Simulation

In this section, we apply the aforementioned concept to SiDB-based gates to simulate the operating temperature range at which they compute the correct output (for a given input) with a given confidence level. As a first step, we differentiate types of excited states that can influence the computed output, and thus increase the probability of obtaining incorrect gate outputs. Afterwards, the *Critical Temperature* is introduced, which is yielded by the simulator. In general, SiDB-based gates exhibit several physically valid charge configurations with different electrostatic potential energies. The state with the lowest electrostatic potential energy is called the *ground state*, in addition to the *excited states* with higher energy levels. Excited states can exhibit two types of deviations from the ground state: 1) the charge distribution within the gate is different, but the output bits are unaffected; and 2) output bits are affected by the deviation.

In the first case, the gate still computes the correct output for the given input. Therefore, we call this type of excited state *transparent*, in the sense that its population does not lead to visible changes in the gate operation. On the other hand, in the second case, which we call *erroneous*, the gate no longer performs the desired computation. Hence, the population of this type of excited state leads to visibly faulty behavior. In addition to the ground state shown in Fig. 2a, the Figs. 2b and 2c depict the first and second physically valid excited state charge distributions (under the input `10`). In Fig. 2b, the excitation has a visible effect on the output bit, which deviates from the ground state. In Fig. 2c, the left input bit is altered to represent a logic `0`, which is then, however, correctly propagated through the gate leading to a consistent, yet faulty, output of logic `0`. Therefore, both excited states are *erroneous*. Thus, this gate works as intended when assuming its ground state, but starts to fail with the population of its excited states.

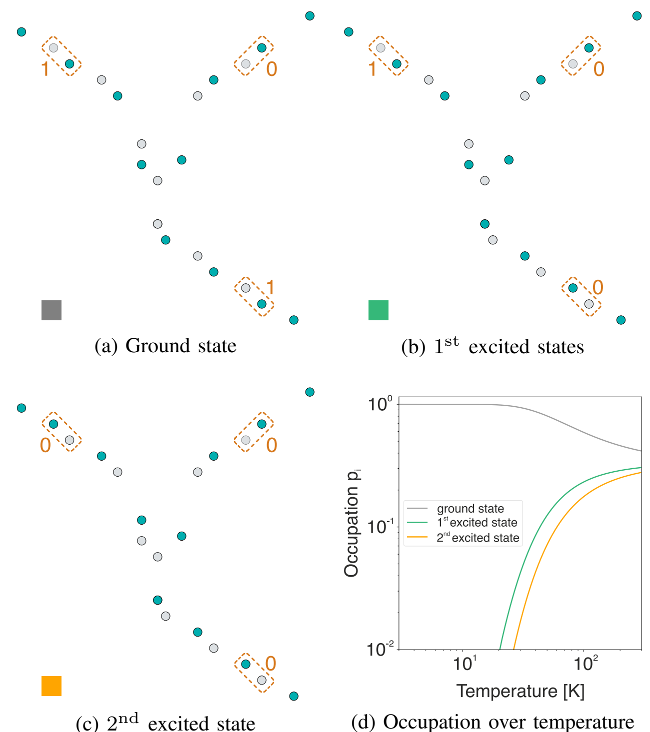


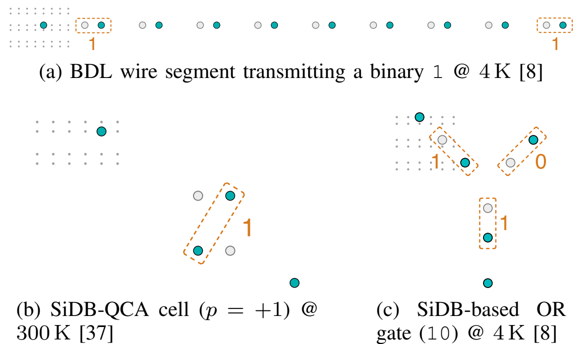
Fig. 2: Physically valid charge configurations of an SiDB-based OR gate [18] with input `10` for the ground state.

Applying Eq. (4) from the previous section, the occupation probability of all three states is plotted against the temperature in Kelvin (K) in Fig. 2d. It can be found that the electrostatic potential energy difference of the physically valid states is only a few meV. Hence, the 1st and 2nd erroneous excited states are already occupied more than $1\,\%$ of the time at $20.2\,\mathrm{K}$ and $26.5\,\mathrm{K}$, respectively.

The temperature that results in a population of *erroneous* excited states with a probability greater than $1-\eta$, where η is the confidence level for the presence of a working SiDB-based gate at a specific input pattern (e. g. `10`), is called the *Critical Temperature* (CT). The CT of an SiDB-based gate is defined as the lowest critical temperature among all distinct input patterns. This value is yielded by the simulator.

IV. Experimental Evaluations

This section constitutes the main contribution of this work. We analyze the temperature behavior of established SiDB-based gate libraries from the literature by determining the CT with the simulator. To this end, we cover three complementary SiDB sets, namely: 1) fabricated SiDB-based gates [8], [37], 2) the *SiQAD* gate library [16], and 3) the *Bestagon* gate library [18]. The experimental setup used in all scenarios is first described in Section IV-A. Afterward, all scenarios are described in Section IV-B to Section IV-D. Finally, the results obtained are summarized in Section IV-E and discussed in Section IV-F.



(a) BDL wire segment transmitting a binary `1` @ 4 K [8]

(b) SiDB-QCA cell ($p = +1$) @ 300 K [37]

(c) SiDB-based OR gate (`10`) @ 4 K [8]

Fig. 3: Recreated measurement results of physically fabricated SiDB layouts.

A. Experimental Setup

For an exhaustive evaluation of the temperature behavior of the three mentioned SiDB sets, the simulator discussed in Section III was implemented in C++ on top of the *fiction*[1] framework [38] which is part of the *Munich Nanotech Toolkit* (MNT). It was applied to determine the CT by passing it all physically valid charge states computed by the exact *ExhaustiveGS* (ExGS) algorithm developed by Ng *et al*. [20]. For the entire evaluation, η was set to 99 %.

B. Fabricated SiDB-based Gates

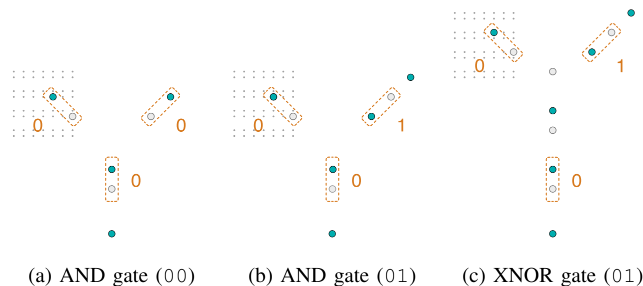
In a first series of investigations, we considered SiDB-based gates that have been manufactured in lab studies and experimentally characterized by Taucer *et al*. [37] and Huff *et al*. [8]. Determining their CT is crucial to show whether these gates are potential candidates for room temperature applications. Fig. 3a depicts a wire consisting of nine pairs of SiDB with an input of logic `1` (on the left), Fig. 3b presents a *Quantum-dot Cellular Automata* (QCA) cell fabricated from SiDBs with a polarization pattern equal to logic `1`. Lastly, Fig. 3c illustrates an SiDB-based OR gate with an input of logic `10`, representative of all possible inputs.

C. SiQAD Gate Library

In a second series of investigations, we considered the SiDB-based gates of the SiQAD gate library presented by Ng *et al*. [16] due to their similarity to the already manufactured OR gate, but also due to their difference in the number of SiDB and therefore a possible change in CT. Also in these gates, input bits are represented by the positions of charges in SiDB pairs (orange boxes), with a default of logic `0` (Fig. 4a). The gates possess the ability to switch to logic `1` via the placement of input perturbers as depicted in Fig. 4b and Fig. 4c for the AND gate and the XNOR gate, respectively. However, compared to Huff *et al*.'s OR gate [8], which consists of only six SiDBs (without counting perturbers), these newly synthesized gates are slightly larger in area and consist of up to nine SiDBs.

Since these gates were validated using existing simulation algorithms, their temperature behavior is not yet known. Therefore, they are analyzed in this work to reveal their temperature behavior.

[1] `https://github.com/cda-tum/fiction`



(a) AND gate (`00`) (b) AND gate (`01`) (c) XNOR gate (`01`)

Fig. 4: *SiQAD* gates: AND gate with input `00` and input `01` and XNOR gate input `01`.

TABLE I: Critical temperature of fabricated SiDB layouts.

Benchmark [8], [37]			Obtained Results			
Name	#SiDBs	#inst.	CT_{min} [K]	#valid	μ_-	$E_{g,err}^{min}$
Wire	19	1	$> RT$	2	−0.231	—
QCA	6	1	$> RT$	1	−0.320	—
OR	7 – 9	4	$> RT$	4	−0.280	—

D. Bestagon Gate Library

In the final series of investigations, the *Bestagon* gate library [18] was analyzed. It constitutes a collection of uniform hexagonal SiDB standard tiles that have been proposed to circumvent the challenges that prior designs have imposed. Each gate in the Bestagon library occupies the same area and possesses standardized input and output pins as depicted in Fig. 5, which make them particularly suited for the automatic design of large circuitry. Furthermore, tile dimensions have been selected in a way that respects the metal pitch of contemporary CMOS fabrication nodes, which are required for the manufacturing of embedded clocking electrodes.

In this third experimental case study, we investigate the robustness and reliability of the Bestagon gates under realistic conditions, specifically under the influence of the temperature. The obtained data enables a deeper understanding of their behavior in a range of temperature scenarios.

E. Obtained Results

All obtained results are summarized in Table I, Table II, and Table III for scenarios described in Section IV-B, Section IV-C, Section IV-D, respectively. The first three columns provide the name of the gate, the number or range of SiDBs, and the number of simulated layouts (instance count). Next, the CT obtained in Kelvin (K) of the corresponding gate and the number of physically valid charge configurations are listed. In the final column, the minimal energy difference between the ground state (g) and the 1st erroneous excited state (err) $E_{g,err}^{min}$ is stated. For the simulation of the fabricated layouts, different physical values are assumed. Thus, the μ_- is additionally provided in the 6th column of Table I.

F. Discussion

After describing all three scenarios in detail, this section presents the results of the temperature analysis. The results for each of the three scenarios are summarized at the end of each subsection.

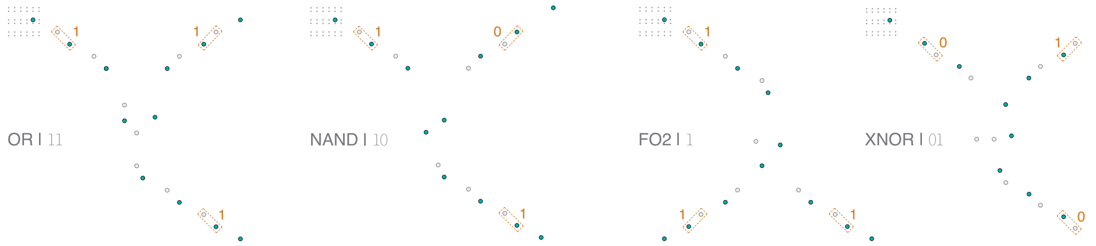


Fig. 5: Ground state results of selected *Bestagon* logic gates with $\mu_- = -0.32\,\mathrm{eV}$, $\epsilon_r = 5.6$, $\lambda_{TF} = 5\,\mathrm{nm}$.

TABLE II: Critical temperature of SiQAD gates.

BENCHMARK [16]			OBTAINED RESULTS		
Name	#SiDBs	#inst.	CT_{min} [K][a]	#valid	$E_{g,err}^{min}$
AND	$7-9$	4	$> RT$	4	—
XOR	$9-11$	4	21.37	7	8.17
XNOR	$10-12$	4	12.19	5	4.66
NAND	$9-11$	4	1.99	6	0.80

[a] $\mu_- = -0.28\,\mathrm{eV}$; $\epsilon_r = 5.6$; $\lambda_{tf} = 5\,\mathrm{nm}$.

TABLE III: Critical temperature of Bestagon gate layouts.

BENCHMARK [18]			OBTAINED RESULTS		
Name	#SiDBs	#inst.	CT_{min} [K][a]	#valid	$E_{g,err}^{min}$
NAND	19	4	92.25	12	34.62
AND	21	4	55.22	22	22.85
XNOR	21	4	45.77	14	18.21
XOR	21	4	35.87	18	13.73
Double Wire	28	4	24.18	65	10.72
NOR	19	4	17.82	18	7.78
Wire diagonal	16	2	6.03	8	2.31
OR	21	4	5.38	19	2.06
Wire straight	15	2	4.89	7	1.87
INV diagonal	18	4	1.59	12	0.61
FO2	20	2	1.46	15	0.56
INV straight	18	2	1.03	17	0.39
CX	27	4	0.85	40	0.32
HA	24	4	0.40	39	0.15

[a] $\mu_- = -0.32\,\mathrm{eV}$; $\epsilon_r = 5.6$; $\lambda_{tf} = 5\,\mathrm{nm}$.

1) Fabricated SiDB-based Gates: The temperature-aware physical simulation shows that Huff *et al.*'s wire segment (Fig. 3a, [8]) is temperature robust, and can therefore operate correctly even at RT and above. Although a kink energy, i. e., the energy required to create a kink, of $9.19\,\mathrm{meV}$ is revealed (which means that an excited state is occupied with a probability greater than $1\,\%$ above $25\,\mathrm{K}$), the output is not affected by the kink and still propagates the input `1` (given by the placed perturber) to the output as illustrated by Fig. 6. Due to this characteristic, the 1st excited state is *transparent* as outlined in Section III-B.

Moreover, temperature-aware physical simulation for both Taucer *et al.*'s QCA cell (Fig. 3b, [37]) and Huff *et al.*'s OR gate (Fig. 3c, [8]) reveals that the temperature does not affect the charge distribution, which can be traced back to the existence of only one physically valid charge state, and hence an infinitely high kink energy.

Fig. 6: The 1st excited state of the BDL wire from Fig. 3a is *transparent*. The perturber on the left indicates a logic `1` input, which is inverted twice, leading to a correct output on the right.

In summary, the temperature analysis shows that this investigated set of already fabricated SiDB-based gates has a high-temperature robustness, which means that these gates can be used without complex and expensive cooling.

2) SiQAD Gate Library: The temperature-aware physical simulation of the SiQAD AND gate yields a CT which is above room temperature. This pronounced temperature robustness can be attributed to the specific arrangement and the number of SiDBs, since Huff *et al.*'s OR gate—after which the SiQAD gates are modeled—also shows a high temperature robustness. In contrast, temperature-aware physical simulation of the other gates in Table II, namely XOR, XNOR, NAND, provides dramatically reduced CT values. This is due to the formation of at least one additional physically valid charge state with an electrostatic potential system energy similar to the ground state ($E_{g,err}^{min} = 8.17\,\mathrm{meV}$, $4.66\,\mathrm{meV}$, $0.80\,\mathrm{meV}$, respectively for the three gates). Since these energy values correspond to less than $35\,\%$ of the thermal energy at RT, a population of these 1st *erroneous* excited states occur already at low temperatures and leads to faulty calculations.

The formation of additional physically valid charge distributions can be the result of the increase in the number of SiDBs, as contrasted in Fig. 4. Hence, an increase in the number of SiDBs can be accompanied by a reduction in the temperature robustness. This must be taken into account when designing future gate libraries.

By analyzing the temperature behavior of the SiQAD gate library, it was shown for the first time that SiDB-based gates can be highly temperature sensitive, which in this case means that low temperatures are required for accurate computation.

3) Bestagon Gate Library: Similar to the SiQAD gate library discussed before, the temperature analysis of gates from the *Bestagon* gate library has also revealed a striking sensitivity to thermal energy, with a CT below $100\,\mathrm{K}$ for all gates. This high sensitivity can be attributed to the elevated number of SiDBs in comparison to previously discussed gates, further emphasizing the crucial nature of considering

temperature in gate library design. CT varies substantially among the different gates, with a range of $0.4\,\mathrm{K}$ for the half-adder to $92.3\,\mathrm{K}$ for the NAND gate. This variation is due to the different energy landscapes of the gates (NAND: $E_{g,err}^{min} = 34.62\,\mathrm{meV}$; HA: $E_{g,err}^{min} = 0.15\,\mathrm{meV}$). Since $E_{g,err}^{min}$ determines to a large extent the population (Eq. (4)) of the 1st *erroneous* excited state as a function of temperature (high energy differences require a high temperature for occupation), it is clear that the Bestagon NAND gate can operate at higher temperatures than the other gates of the same library. The five gates at the bottom of Table III possess a CT even below the temperature of liquid helium ($4.15\,\mathrm{K}$). As they require ultra-low operating temperatures, their usage proves to be challenging.

To reiterate, the low CT values are due to a small energy difference between the ground state and the 1st *erroneous* excited state. All five gates (INV diagonal, FO2, INV straight, CX, HA) show values for $E_{g,err}^{min}$ below $1.9\,\mathrm{meV}$, which corresponds to less than $8\ \%$ of the thermal energy at RT, which means that even at ultra-low temperatures, the thermal energy is sufficient to lead to a population of the excited states. In addition, all five gates exhibit many physically valid charge configurations, which further decreases the CT.

The results of the comprehensive experimental evaluation performed on the Bestagon gates demonstrate their pronounced sensitivity to temperature, as evidenced by the low CT values observed for all gates. This information is crucial for the advancement of the SiDB technology and should be factored into the design automation process by reducing the use of gates with high thermal sensitivity. It is noteworthy that fundamental circuit elements, such as crossings (CX), inverter (INV), and regular wire segments, appear to be particularly vulnerable to thermal noise in the present implementation of the Bestagon gates. However, it is important to keep in mind that this is only true for the gates investigated in this study and may not be an inherent characteristic of these functions. Thus, it is imperative to make efforts to create robust circuit elements that can withstand thermal noise.

V. Conclusions

This study marks a significant milestone in the development of the *Silicon Dangling Bond* (SiDB) technology by presenting the first temperature-aware simulation of SiDB systems. The results of our extensive experimental evaluation demonstrate the pronounced impact of thermal energy on established gates. This highlights the criticality of taking temperature into account when designing SiDB circuits and underscores the need for reducing the use of highly temperature-sensitive gate elements in future designs. Our findings provide crucial insights for subsequent studies in the domain and for design automation flows of SiDB circuitry, thereby furthering the development and advancement of this promising green nanotechnology.

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