Towards Atomic Defect-Aware Physical Design of Silicon Dangling Bond Logic on the H-Si(100)-2×1 Surface

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***Abstract*—Recent advancements in *Silicon Dangling Bond* (SiDB) fabrication have transitioned from manual to automated processes. However, sub-nanometer substrate defects remain a significant challenge, thus preventing the fabrication of functional logic. Current design automation techniques lack defect-aware strategies. This paper introduces an idea for a surface defect model based on experimentally verified defects, which can be applied to enhance the robustness of established gate libraries. Additionally, a prototypical automatic placement and routing algorithm is presented, utilizing STM data from physical experiments to obtain dot-accurate circuitry resilient to atomic surface defects. Initial evaluations on surfaces with varying defect rates demonstrate their critical impact, suggesting that fabrication processes must achieve defect rates of around 0.1 % to further advance this circuit technology.**

I. Introduction & Motivation

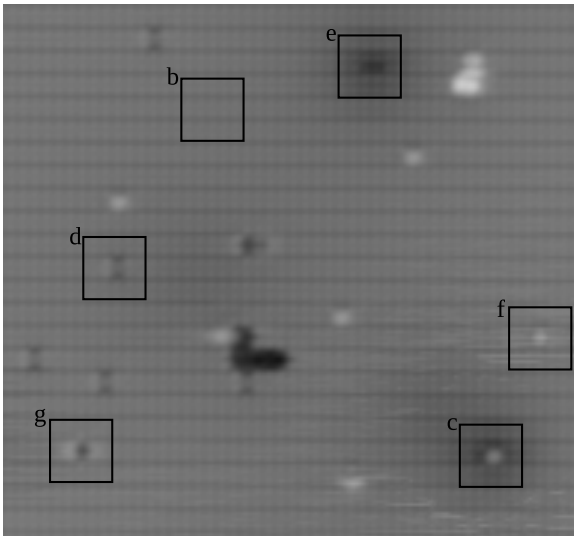
Acting as atomically-sized quantum dots, *Silicon Dangling Bonds* (SiDBs) have seen tremendous recent fabrication advancements, making it an attention-worthy post-CMOS candidate [1]. However, SiDB device fabrication and operation are hampered by the technology's atomic precision requirements which are sensitive to sub-nanometer level substrate defects occurring during hydrogen-passivated silicon (H-Si(100)-2×1) surface preparation [2], [3].

This paper introduces an initial idea for defect-aware SiDB logic, integrating defect analysis into automatic layout design. The main contributions are: 1) Proposing an atomic defect model categorizing 13 types of H-Si(100)-2×1 surface defects to facilitate design automation. 2) Analyzing the *Bestagon* gate library's sensitivity to certain defects and proposing robust redesigns [4]. 3) Developing a prototypical algorithm for placement and routing of SiDB circuit layouts that avoids regions with atomic defects. 4) Estimating the impact of defects on H-Si(100)-2×1 surfaces via initial experiments, providing insights for future large-scale SiDB device fabrication.

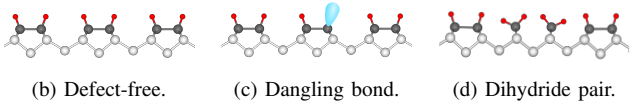
The proposed framework introduces SiDB physical design under defect constraints. Our findings suggest that a defect rate of around 0.1 % cannot be exceeded for large scale SiDB circuit manufacturing. Overall, this motivates the development of dedicated defect-aware design frameworks.[1]

II. Atomic Surface Defects

Contemporary H-Si(100)-2×1 surfaces posses an unavoidable concentration of atomic defects, deviations from the ideal surface phase, such as unpassivated or missing silicon atoms, contaminant atoms, or structural deformation. These variation effect uniform SiDB creation, SiDB behavior, and logic gate functionality.



(a) STM surface scan of 19 nm × 18 nm with visible defects.



(b) Defect-free. (c) Dangling bond. (d) Dihydride pair.

(e) Silicon vacancy. (f) Siloxane dimer. (g) Missing dimer.

Fig. 1: A H-Si(100)-2×1 surface and common atomic defects found thereon depicted as side-view ball-and-stick models.

Fig. 1a shows an STM scan of a fabricated H-Si(100)-2×1 surface with a variety of highlighted defects corresponding to the ball-and-stick-model depictions in Fig. 1b to Fig. 1g [2].

This work addresses the atomic defect gap in SiDB logic and design automation research, thus preventing further fabrication infeasibility stemming from defect-agnostic layout design.

[1] A supplementary repository containing all surface data and the initial implementation of the prototypical physical design algorithm is publicly available at `https://github.com/cda-tum/sidb-defect-aware-physical-design`.

TABLE I: Layout data obtained from physical design on experimentally fabricated and simulated H-Si(100)-2×1 surfaces.

Benchmark [4]			Examined Surface Data															
			Experimental STM Scans				Simulated w/ Charged Defects						Simulated w/o Charged Defects					
	defect-free		8.57 % defective		6.26 % defective		1 % defective		0.5 % defective		0.1 % defective		1 % defective		0.5 % defective		0.1 % defective	
Name	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]	#SiDBs	A[nm^2]
xor2	59	979.55	—	—	—	—	58	1120.67	59	979.55	58	1120.67	59	1268.12	59	979.55	59	979.55
xnor2	63	979.55	—	—	—	—	62	1120.67	63	979.55	62	1120.67	63	1268.12	63	979.55	63	979.55
par_gen	99	1956.15	—	—	—	—	—	—	97	2094.47	111	1882.72	98	1898.50	98	1956.15	98	1956.15
mux21	177	3447.67	—	—	—	—	—	—	—	—	230	5540.22	—	—	163	3842.41	179	5533.14
par_check	317	6051.59	—	—	—	—	—	—	—	—	358	7924.58	—	—	382	20 899.23	229	6577.13
xor5_r1	200	3447.67	—	—	—	—	—	—	216	7524.68	174	4682.02	—	—	198	5629.58	210	3941.50
xor5_majority	191	3445.16	—	—	—	—	—	—	209	7524.68	166	4682.02	181	5533.14	205	5629.58	257	5926.85
t	459	7924.58	—	—	—	—	—	—	—	—	443	8724.82	—	—	541	20 502.28	424	9768.67
t_5	482	7924.58	—	—	—	—	—	—	—	—	458	8941.14	—	—	487	17 122.00	436	10 416.59
c17	341	6330.29	—	—	—	—	—	—	—	—	391	7924.58	—	—	598	20 577.78	466	10 316.02

III. Defect-Aware Physical Design

This section proposes an idea for an SiDB logic framework that can address the limitations of current methods in handling atomic surface defects.

A. Surface Defect Model & Robust Gate Library

Defect-aware design begins by the identification of defect charge, which is enabled by a pixel-based defect-type classification from STM images using a CNN based on [5].

An initial idea is established to determine the minimum distance for gate tiles from defects to maintain correct logic operation, involving physical simulations [6]–[8] and experimentally fitted parameters for silicon vacancy defects [3]. This process is applied to the *Bestagon* standard gate library [4], identifying nonfunctional tiles at tested defect distances. Subsequently, tiles are redesigned using an automated SiDB layout designer based on reinforcement learning [9], aiming for minimal avoidance distances.

B. Automatic Physical Design

Our idea is to adopt tile-based design, assuming a hexagonal tiling with established SiDB gates [4], [10], yet to remain applicable to any tiling and standard library. Differing from idealized defect-free surface assumptions, we incorporate realistic STM scans as input. Overlaying a tiling, each gate and wire is matched against each tile in every rotation, identifying defective gate-tile pairs to construct a blacklist.

This blacklist, comprising SiDB structures unable to function correctly on specific tiles, is used as a set of constraints in a satisfiability-based placement and routing algorithm [11]. The algorithm ensures these gates/wires are not placed on the affected tiles, resulting in a navigation around surface defects, thereby maintaining functionality despite disturbances.

IV. Experimental Evaluation

In this section, we present and discuss initial results of an experimental evaluation of the proposed concepts by the means of Table I.

A. Experimental Setups

Two surfaces were experimentally fabricated and measured with an STM, supplemented by simulations. STM measurements utilized an Omicron LT-STM system at $4.5\,\mathrm{K}$ and $3 \times 10^{-11}\,\mathrm{Torr}$ vacuum. Images were acquired in constant height mode using a Nanonis SPM controller.

A CNN for defect identification, based on [5], was implemented in Python using Keras and TensorFlow, expanding the training data and increasing the defect classes to 13. The prototypical defect-aware placement and routing algorithm was implemented in C++ for the *Munich Nanotech Toolkit* (MNT) *fiction* [12].

B. Results

The obtained STM scans showed defect rates of $8.57\,\%$ and $6.26\,\%$ on fabricated H-Si(100)-2×1 surfaces. The defect-aware algorithm applied to benchmark circuits indicated no successful layout generation due to high defect rates, emphasizing the impact of atomic defects on logic design [13]. Simulated surface evaluations with variable defect rates ($1\,\%$, $0.5\,\%$, $0.1\,\%$) hint at three key findings: 1) increased area consumption due to defect avoidance, 2) substantial impact of high defect rates and charged defects on layout feasibility, 3) and the necessity of achieving a defect rate around $0.1\,\%$ for larger-scale layout manufacturing.

V. Conclusions

This work addresses the challenges of atomic substrate defects in *Silicon Dangling Bond* (SiDB) fabrication. We developed a surface defect model from 13 H-Si(100)-2×1 defect types to enhance SiDB gate library robustness and introduced a prototypical defect-aware placement and routing algorithm operating on STM data. Initial results highlight the necessity of limiting defect rates to around $0.1\,\%$, particularly in the presence of charged defects, to advance SiDB logic manufacturing. Overall, this motivates the development of dedicated defect-aware design frameworks.

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