Unifying Figures of Merit: A Versatile Cost Function for Silicon Dangling Bond Logic

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https://www.cda.cit.tum.de/research/nanotech/

***Abstract*— As *Silicon Dangling Bond* (SiDB) logic emerges as a promising beyond-CMOS technology, Figures of Merit (FoMs) to assess gate performance become crucial in implementing devices that are robust against environmental variations. Constructing robust SiDB logic involves designing gates that excel across multiple FoMs. However, there exist no clear guidelines on the ideal ranges for FoM values, nor a systematic approach to designing SiDB gates that optimize across multiple FoMs. Motivated by this, this work focuses on addressing the following key objectives: 1) Introduction of a new FoM, called *Band Bending Resilience*. 2) Determination, presentation, and detailed discussion on the best achievable values for each FoM for all 2-input Boolean functions. 3) Presentation of the versatile cost function χ, unifying multiple FoMs tailored to specific application requirements and priorities. 4) Implementation of the optimization strategy using the cost function χ, which aims at designing SiDB logic with minimal cost, ensuring an optimal balance between all FoMs. Overall, this research contributes significantly to the understanding of SiDB logic, establishing a basis for future progress in the field.**

I. Introduction

The 2023 Nobel Prize in Chemistry celebrated the groundbreaking discovery and synthesis of quantum dots, underscoring the profound significance and potential of nanotechnology [1], [2]. Whereas traditional quantum dots which have been under investigation for decades often compose of several thousand atoms, the emergence of *Silicon Dangling Bonds* (SiDBs) herald the arrival of quantum dots at the single-atom scale, with the capability to implement beyond-CMOS computing devices [3]–[8]. These SiDBs can be precisely manufactured on the spatially periodic H-Si(100)-2×1 surface using a *Scanning Tunneling Microscope* (STM, [4]). SiDBs posses the capability to maintain negative, neutral, or positive charge states; these discrete states can be manipulated when multiple SiDBs exist in close proximity, facilitated by electrostatic field coupling. These unique properties have been successfully exploited for constructing logic gates and wire segments [3], [4].

The revolutionary SiDB logic platform has attracted considerable attention, leading to rapid advancements in a set of highly efficient physical simulators, including *QuickSim* [9], *QuickExact* [10], and *SimAnneal* [11]. Moreover, design automation capabilities and gate libraries have already been proposed in the literature [12]–[16]. The availability of these tools accelerates the exploration of novel SiDB logic designs.

Recent efforts have focused on creating tools and Figures of Merit (FoMs) to evaluate the robustness of SiDB logic. A temperature-aware simulator for SiDB logic was presented [17]. Moreover, several operational domain algorithms for assessing sensitivity to changes in physical parameters and a systematic workflow for testing logic gate robustness to charged defects were proposed [18], [19]. However, there exist no clear guidelines on the ideal ranges for FoM values, nor a systematic approach to designing SiDB gates that optimize across multiple FoMs.

Motivated by this, this work focuses on addressing the following key objectives:

1) Introduction of a new FoM, called *Band Bending Resilience*.
2) Determination, presentation, and detailed discussion on the best achievable values for each FoM for all 2-input Boolean functions.
3) Presentation of the versatile cost function χ, unifying multiple FoMs tailored to specific application requirements and priorities.
4) Implementation of the optimization strategy using the cost function χ, which aims at designing SiDB logic with minimal cost, ensuring an optimal balance between all FoMs.

The remainder of this work is structured as follows: Section II reviews the SiDB logic platform. Subsequently, Section III summarizes common FoMs from the SiDB literature and proposes the novel *Band Bending Resilience* as a FoM. In Section IV, the versatile cost function χ is formulated for the first time, and an algorithm for designing gates that minimize χ is introduced. In Section V, first, an exhaustive analysis of the best possible FoM values is conducted. Second, the proposed strategy is used to design gates that minimize χ and thus satisfy the best trade-off between all individual FoMs. Finally, Section VI provides a summary of the key findings and contributions of this work.

II. The SiDB Logic Platform

SiDBs are typically created using an atomically sharp tip of a *Scanning Tunneling Microscope* (STM) [4], [6], [20]–[22]. By applying a voltage at the STM tip, the hydrogen atom is desorbed from the surface, leaving behind an open valence bond (sp^3-orbital) called an SiDB.

Each SiDB can accommodate up to two electrons [23]. The number of electrons within the SiDB, and thus its charge state, depends on the local electrostatic potential, which can be caused by, for example, external electrodes or neighboring

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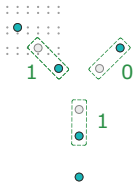
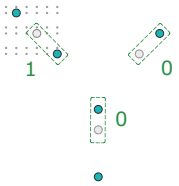
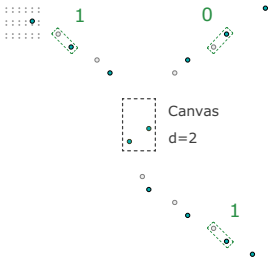
(a) BDL wire consisting of three pairs. A perturber on the left exerts an electrostatic potential, simulating a binary `1` input.



(b) SiDB OR gate with input pattern `10` [3], [11].



(c) SiDB AND gate with input pattern `10` [11].



(d) *Bestagon* NAND gate with input pattern `10` [13]. The *Canvas* is represented as dashed box.

Fig. 1: The SiDB logic platform.

SiDBs. This ability to exhibit discrete charge states while being isolated from the conduction band is essential for constructing logic gates and devices [3], [4], [23]. This pioneering research has led to the successful fabrication of wires consisting of *Binary-Dot Logic* (BDL) pairs [3], [4]. As a pivotal demonstration of SiDB logic, gates with a footprint smaller than $30\,\mathrm{nm}^2$ [3] have been successfully manufactured.

Example 1: In Fig. 1a, an SiDB wire is depicted, comprising three BDL pairs highlighted by dashed green rectangles. The single SiDB on the left, referred to as a *perturber*, exerts Coulombic pressure on the pairs, thereby propagating a binary `1` signal through the wire. Leveraging the same BDL principle, logic gates can be realized, exemplified by the OR and AND gates in Fig. 1b and Fig. 1c respectively. Additionally, Fig. 1d showcases the *Bestagon* NAND gate with input pattern `10` as described in [13] with two input and one output wire. The NAND logic is achieved through the specific arrangement of the two SiDBs in the *Canvas* (an area designated for SiDB placement).

III. FoMs for SiDB Logic

FoMs are important for evaluating device performance and comparing the quality of different devices. In SiDB logic, FoMs are particularly important for gauging robustness. This section reviews and introduces a range of different FoMs aimed at providing comprehensive insight into gate robustness. In addition, it is shown that gate implementations which perform well on one FoM often suffer on others, underscoring the challenge of designing gates that excel on all FoMs.

A. Critical Temperature (CT)

At the nanoscale, energy differences between excited states are typically in the meV range, where thermal noise significantly affects the physical behavior of the system [17]. Recent research underscores the importance of considering thermal effects in SiDB logic [17]. The temperature simulator presented in this context provides the CT, which indicates the temperature at which the analyzed gate's reliable operational behavior ceases. To avoid expensive cooling, a high CT is preferred.

B. Operational Domain (OPD)

Apart from dealing with thermal noise, SiDB logic is sensitive to substrate material-specific parameter variations caused by manufacturing imprecision. Particularly the *relative permittivity* ϵ_r and the *Thomas-Fermi screening length* λ_{tf} are impacting electrostatic interactions. The OPD assesses the SiDB logic gate's tolerance to these variations [11], [18], [19], [24]. To be less sensitive to variations in these physical parameters, large values for the OPD are preferred.

C. Minimum Defect Clearance (MDC)

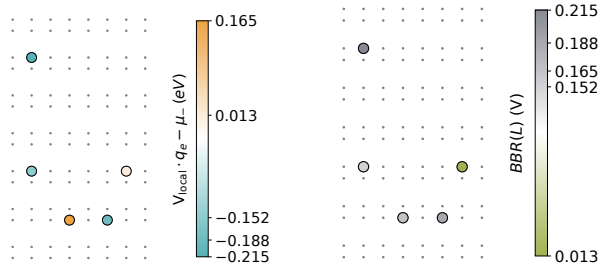
Since SiDB logic relies on electrical field coupling, it is critical to recognize the significant impact of ambient electrostatic influences on the behavior of a gate. Atomic defects, both charged and neutral, commonly occur on the H-Si(100)-2×1 surface with state-of-the-art manufacturing techniques [8], [21], [25], [26]. To assess how sensitive a given gate is to charged atomic defects, the MDC method has been proposed by [19], which describes the minimum distance the gate must keep from any atomic defect to ensure operability. Therefore, a low value for the MDC is preferable.

D. Band Bending Resilience (BBR)

As emphasized earlier, SiDBs can be either negatively, neutrally, or positively charged depending on the local electrostatic potential at their location, denoted $V_{local,i}$, and μ_-, which describes the energy difference between the *Fermi Energy* and the charge transition level $(0/-)$. If $V_{local,i} \cdot q_e$ ($q_e = -e; e =$ *elementary charge*) is close to the value of μ_-, even small perturbations can cause a charge state flip. Conversely, for SiDBs where the local electrostatic potential differs significantly from μ_-, larger perturbations are required for a charge flip induced by band bending (i. e., charge change is not due to electron hop between two SiDBs). The latter case is desirable for stable and robust charge configurations.

To analyze this phenomenon quantitatively, this work introduces the BBR as a respective FoM. This FoM represents the minimum electrostatic potential required to induce a charge change in one of the SiDBs due to electrostatic band bending. Therefore, high values are desirable for robust SiDB logic.

Example 2: Consider the SiDB layout depicted in Fig. 2a, showcasing the charge distribution of the ground state. The color bar illustrates the difference between $V_{local,i} \cdot q_e$ and μ_-. Negative values, depicted in blue, signify negatively charged SiDBs, while positive values suggest neutrally charged SiDBs (under the assumption that the interaction is insufficient to induce positively charged SiDBs). This assumption holds under the condition that the SiDBs are separated by more than one lattice position.



(a) Local electrostatic potential landscape for $\epsilon_r = 5.6$, $\lambda_{tf} = 5\,\mathrm{nm}$, $\mu_- = -0.32\,\mathrm{eV}$.

(b) $BBR(L)$

Fig. 2: Electrostatic potential landscape and BBR values for all SiDBs of the layout L.

In this layout, three SiDBs are negatively charged (shown in blue), indicating that a significant local electrostatic potential is required to change their charge state to neutral. Consequently, these three SiDBs exhibit high BBR values (as shown in Fig. 2b), denoting their robustness. Conversely, the remaining two SiDBs in Fig. 2a are neutrally charged. Notably, the SiDB positioned farthest to the right demonstrates $V_{local,i} \cdot q_e \approx \mu_-$, implying even a minor alteration in the electrostatic potential could trigger a transition to a negative charge state. In this specific instance, the BBR is $0.013\,\mathrm{V}$ $(13.0\,\mathrm{mV})$, indicating a high sensitivity to external influences.

E. Analyzing the Trade-off between Various FoMs

Designing gates that achieve best possible values across all FoMs poses a challenge due to the absence of a straightforward connection between them as shown in Example 3.

Example 3: Assume an AND gate with the maximum CT is to be selected from all possible implementations with $d = 3$ from [27]. The maximum CT is $138.28\,\mathrm{K}$. This gate implementation yields an OPD of $5.0\,\%$. However, opting for the gate with the maximum OPD, which is $22.0\,\%$, results in a CT of only $0.81\,\mathrm{K}$. Additionally, the Pearson correlation coefficient between CT and OPD is calculated as -0.44, indicating a weak negative correlation. This highlights the intricate trade-off required when optimizing the FoM values.

Thus, relying on a simplistic approach to gate design, which focuses on optimizing one FoM while hoping for favorable outcomes in others, is futile (Example 3). Designers must strike a balance and make informed decisions based on the specific requirements and priorities of the application or system in which the gate will be used. To achieve this goal, the versatile cost function χ is presented in the following section to address this challenge, which is an important contribution of this work.

IV. Optimizing Gate Robustness with the Cost Function χ

Designing a gate that simultaneously achieves the best possible values for all FoMs is, in most cases, not feasible. Instead, a trade-off must be made between the individual FoMs. However, the importance of each FoM varies depending on the specific application and environment in which the SiDB logic is deployed.

To design SiDB gates that excel across multiple FoMs while also accommodating user-defined priorities for specific FoMs, we introduce a novel approach that unifies an arbitrary number of FoMs using the versatile cost function χ. This method allows for a comprehensive evaluation of gate robustness while offering flexibility in prioritizing specific FoMs based on the users' requirements and preferences via individual weighting. In addition, we present an algorithm that designs gates based on these specified weights, aiming to minimize the overall cost and achieve the optimal trade-off. This makes it possible, for the first time, to design robust gates over multiple FoMs while incorporating user-defined prioritization of the individual FoMs.

The cost function χ is first introduced in Section IV-A, describing its importance in unifying several FoMs. Then, in Section IV-B, the implementation details of the algorithm for designing optimal gates based on the cost function χ are presented and discussed in detail.

A. Cost Function χ

Considering an arbitrary number of FoMs, the versatile cost function χ of an SiDB layout L is defined as follows:

$$\chi(L) = \sum_i w_i \cdot \chi_i(L), \text{ where } \chi_i(L) = \frac{C_i(L)}{C_{i_{\max}}} \tag{1}$$

$\chi(L)$ is the sum of the normalized costs for each FoM ($\chi_i(L)$), weighted by their respective importance (w_i). Each normalized cost $\chi_i(L)$ is calculated by dividing the actual cost $C_i(L)$ of the i-th FoM in the layout L by the maximum possible cost $C_{i_{\max}}$ for that FoM.

The following assignment is undertaken using the previously introduced FoMs: $C_1(L) = -CT(L)$, $C_2(L) = -OPD(L)$, $C_3(L) = -BBR(L)$, $C_4(L) = MDC_{arsenic}(L)$, $C_5(L) = MDC_{vacancy}(L)$. The weights $w_i \in \mathbb{R}_+$ are adjustable, reflecting the importance of specific FoMs for a given use case. It is important to note that C_1, C_2, and C_3 are expressed with negative signs, indicating that larger values of these FoMs are preferable. Conversely, C_4 and C_5 have positive signs, highlighting the importance of keeping these values small. In subsequent discussions, χ_{custom} denotes the cost function corresponding to this customized assignment of cost functions.

Example 4: Assume an SiDB layout L designed to function as a valid gate implementation for the Boolean AND function. Analyses revealed the CT to be $40.7\,\mathrm{K}$, with the maximum temperature CT_{max} set to $400\,\mathrm{K}$. Additionally, the operational domain $OPD(L)$ is measured to be $20\,\%$, while the defect clearance distance for arsenic and silicon vacancy defects are $MDC_{vacancy} = 10.2\,\mathrm{nm}$ and $MDC_{arsenic} = 5.2\,\mathrm{nm}$, respectively. The maximum defect clearance distances are $MDC_{max,arsenic} = 7.2\,\mathrm{nm}$ and $MDC_{max,vacancy} = 12.2\,\mathrm{nm}$. Furthermore, the BBR value $BBR(L)$ is recorded as $5.0\,\mathrm{mV}$, with the maximum achievable $BBR_{max}(L) = 10.0\,\mathrm{mV}$. Assuming a specific use case where atomic defects are considered less critical and therefore assigned a lower weight ($w_{vacancy}, w_{arsenic} = 0.1$), while all

Algorithm 1: Cost-Driven Gate Design

Input: Boolean function $f : \mathbb{B}^n \to \mathbb{B}^m$ to implement
Input: Gate skeleton K with canvas
Input: Upper bound of canvas SiDBs $d_{\max}$
Input: Physical simulation parameters $P = \{\mu_-, \lambda_{tf}, \epsilon_r\}$
Input: Cost function χ_{custom} to optimize
Output: Tuple of the optimum gate layout and its associated cost value

1 $(g^*, c^*) \leftarrow (\emptyset, \infty)$
2 **for** $d = 1 \dots d_{\max}$ **do**
3 $\quad Gates \leftarrow$ *Auto. Exhaustive Gate Designer*(f, K, P, d) // [27]
4 $\quad$ **foreach** $g \in Gates$ **do**
5 $\quad\quad$ **if** $\chi_{custom}(g) < c^*$ **then**
6 $\quad\quad\quad (g^*, c^*) \leftarrow (g, \chi_{custom}(g))$
7 $\quad\quad$ **end if**
8 $\quad$ **end foreach**
9 **end for**
10 **return** (g^*, c^*)

other FoMs are equally weighted ($w_i = 1.0$), the cost of the layout is computed as $\chi_{custom}(L) = -1.0 \cdot \frac{40.7\,\mathrm{K}}{400\,\mathrm{K}} - 1.0 \cdot 0.2 - 1.0 \cdot \frac{5.0\,\mathrm{mV}}{10.0\,\mathrm{mV}} + 0.1 \cdot \frac{5.2\,\mathrm{nm}}{7.2\,\mathrm{nm}} + 0.1 \cdot \frac{10.2\,\mathrm{nm}}{12.2\,\mathrm{nm}} \approx -0.65$, while the theoretical optimum is $\chi_{custom,min} \approx -3.0$.

B. Implementation Details

To design gates that minimize χ_{custom}, several steps are conducted. Initially, as many gate implementations as possible are designed for a given Boolean function. These designs then undergo physical simulations to assess various FoMs. Subsequently, these FoM values are used to calculate the corresponding cost value χ_{custom}. Finally, the gate with $\chi_{custom,min}$ is selected and returned.

The process is detailed in Algorithm 1. It receives as input a Boolean function f, a suitable gate skeleton K with a canvas, the maximum number of SiDBs $d_{\max}$ allowed in the canvas, physical simulation parameters P, and a cost function χ to optimize. In Line 2, the algorithm initializes $d = 1$ and designs all gate implementations with one canvas SiDB using the *Automatic Exhaustive Gate Designer* [27]. Subsequently, it computes the cost of each gate based on the provided cost function χ_{custom}. If the resulting cost of gate g is superior to that of the previous best gate g^*, the new minimum cost χ^* is updated along with g^* in Line 6. This process repeats until $d_{\max}$ is reached. Finally, in Line 10, the gate implementing f with the lowest cost according to χ_{custom} is returned together with its associated cost value. Since this is an exact algorithm, it is always guaranteed to find the optimum, which is one of the main goals of this work.

To support open research, the implementation is available in the *fiction*[1] framework which is part of the *Munich Nanotech Toolkit* (MNT, [28]).

V. FoM Analysis for SiDB Logic

The primary contribution of this work is twofold. First, it involves a comprehensive determination of the best possible FoM values that can be achieved individually. This provides insight into real-world scenarios where SiDB logic can be effectively employed. These attainable values are also required for normalization in Eq. (1). Second, it involves the novel design of gates with Algorithm 1 that show the best-off between all FoMs, thereby minimizing the cost function χ_{custom}. As a result, these gates represent the most robust designs achievable.

[1]Available at: `https://github.com/cda-tum/fiction`

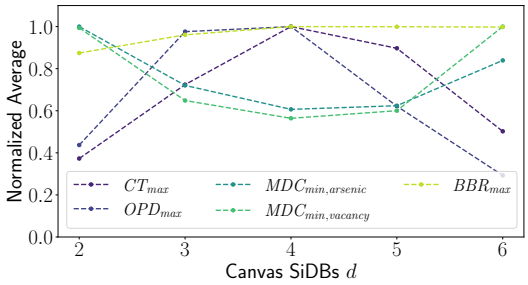


Fig. 3: The average optimal FoM values are computed over all 2-input Boolean functions with different numbers of canvas SiDBs, as shown in the last row of Table I. For CT_{max}, OPD_{max}, and BBR_{max}, the optimization involves maximizing these values, while for *MDC*, minimization is sought.

In Section V-A, the best possible FoM values are determined, presented, and discussed. Afterward, in Section IV, the gates that minimize χ_{custom} are designed and the minimal cost values $\chi_{custom,min}$ are discussed.

A. Determining the Best Possible Values of all FoMs

Before attempting to design robust gates (i. e., those that perform well across multiple FoMs) and thereby minimize the cost function χ_{custom}, this section identifies the best possible values for each introduced FoM. To reiterate, this effort is intended to provide valuable insight into the best possible FoM values for SiDB logic and to enable normalization in χ_{custom}.

To determine the best possible FoM values, the following steps are conducted, which are similar to the steps conducted in Algorithm 1, albeit without incorporating the concept of a cost function: First, all gate implementations for the given Boolean functions are designed using the *Automatic Exhaustive Gate Designer* [27]. Second, for each designed gate, all FoMs are determined. The overall best possible value for each FoM is then identified. Due to the variability in gate design regarding the number of canvas SiDBs, this process is conducted across a range of different values for d. This results in over 29 000 distinct gate designs, for which all FoMs are evaluated.

Table I presents this data for all 2-input Boolean functions. Each section corresponds to a different value of d, ranging from 2 to 6. For each d, the best possible values for all FoMs are listed. Furthermore, the *Average* row presents the mean of the best FoM values across all functions.

Example 5: Exploring the implementation of the NAND function with $d = 4$, we observe the best possible values for CT and OPD at $400.00\,\mathrm{K}$ and $47\,\%$, respectively. However, these values belong to two different gate implementations—both representing the NAND function but differing in the arrangement of the d SiDBs within the canvas.

1) Discussion of the Results: Several key messages can be extracted from the best possible FoM values in Table I, which are discussed below.

TABLE I: Exploring the best possible (CT_{max} in K, OPD_{max} unitless, MDC_{min} in nm, BBR_{max} in mV) and average values of all FoMs across various numbers of d SiDBs for all 2-input Boolean functions. The skeleton and canvas from Fig. 1d are used.

Gate	$d=2$					$d=3$					$d=4$					$d=5$					$d=6$				
	CT	*OPD*[a]	*MDC*[b]		*BBR*	*CT*	*OPD*	*MDC*		*BBR*	*CT*	*OPD*	*MDC*		*BBR*	*CT*	*OPD*	*MDC*		*BBR*	*CT*	*OPD*	*MDC*		*BBR*
			ars[c]	vac[d]				ars	vac				ars	vac				ars	vac				ars	vac	
AND	3.65	0.47	5.17	8.63	40.90	103.61	0.37	2.22	3.44	88.23	112.53	0.39	1.83	3.43	94.73	112.53	0.26	1.80	3.43	104.32	102.40	0.15	2.31	5.79	41.77
NAND	155.63	0.08	3.08	5.00	89.91	400.00	0.49	2.34	4.01	90.84	400.00	0.47	2.31	3.43	126.52	400.00	0.36	2.17	3.43	126.98	229.23	0.03	3.85	4.74	27.48
OR	74.43	0.15	4.86	9.28	77.99	133.73	0.34	1.93	3.84	94.80	156.92	0.41	1.76	2.17	108.19	137.00	0.37	1.76	3.17	124.34	132.12	0.20	1.83	3.39	94.24
NOR	114.09	0.13	3.08	5.43	90.63	227.02	0.34	2.78	4.63	90.84	400.00	0.28	2.74	4.62	109.90	400.00	0.04	3.70	6.68	90.92	-	-	-	-	-
XOR	125.18	0.04	4.86	10.86	90.90	138.28	0.22	4.29	5.85	90.84	132.70	0.26	2.43	4.01	88.11	131.31	0.28	2.37	4.01	84.61	-	-	-	-	-
XNOR	–	–	–	–	–	47.89	0.04	5.05	8.63	89.37	88.92	0.13	3.54	7.56	41.57	88.92	0.13	3.50	5.81	90.92	49.11	0.01	7.00	17.99	26.87
LT	85.28	0.13	5.00	9.62	89.50	85.28	0.34	4.01	5.17	90.12	251.25	0.47	3.42	4.29	84.35	99.02	0.27	2.87	5.05	96.50	-	-	-	-	-
GT	121.53	0.14	4.01	9.35	91.11	210.63	0.24	4.01	6.93	91.11	210.63	0.23	3.54	6.21	87.44	121.18	0.20	2.78	4.74	104.20	-	-	-	-	-
LE	114.09	0.13	3.07	5.43	90.63	227.02	0.34	2.78	4.62	90.84	400.00	0.28	2.74	4.62	109.90	400.00	0.04	3.69	6.68	90.92	-	-	-	-	-
GE	63.08	0.04	7.08	7.74	90.12	275.51	0.53	2.77	4.62	91.11	400.00	0.41	2.80	4.62	125.64	400.00	0.12	3.23	4.87	91.56	-	-	-	-	-
Average	95.22	0.15	4.47	7.93	83.52	184.90	0.33	3.22	5.17	90.81	255.30	0.33	2.71	4.50	97.64	228.97	0.21	2.79	4.79	100.53	128.22	0.10	3.75	7.98	47.59

[a]OPD is determined within $4.0 \leq \epsilon_r, \lambda_{tf} \leq 6.0$ (λ_{tf} in nm)
[b]MDC values are determined using a heuristic approach
[c]arsenic defect
[d]vacancy defect

a) SiDB Logic Can Operate at Room Temperature: For the first time, SiDB logic gates which can operate at room temperature have been successfully modelled. While the state-of-the-art *Bestagon* SiDB gates only operate at below 100 K [17], it is shown that SiDB gates can be designed with significantly higher temperature robustness.

b) Influence of d on the FoM Values: The best possible FoM values closely depend on d as illustrated by the following example.

Example 6: In the case of the NOR gate with $d = 2$, CT_{max} and OPD_{max} are 114.09 K and 13.0 %, respectively. In contrast, at $d = 4$, these values jump to 400.00 K and 28.0 %, denoting more favorable values. This underscores the profound effect of d on the FoM values. In other words, while for $d = 2$ the most temperature-robust gate requires massive cooling down to 114.09 K to enable error-free operation, with four SiDBs in the canvas, an implementation exists that can operate at room temperature.

The relation between the FoM values and d is also illustrated in Fig. 3.

Notably, the FoM values are worse for $d = 2$ and $d = 6$ compared to intermediate values of d. Consequently, achieving good FoM values requires careful consideration of d. Hence, it is crucial to avoid having too few or too many canvas SiDBs, as both scenarios prove disadvantageous, providing an important takeaway for gate design.

c) Individual Gates Do Not Achieve the Best Possible Values Across All FoMs: Attaining the best possible value in one FoM does not ensure its achievement in others, as previously discussed and further underscored by Example 7.

Example 7: The CT and OPD values of all 326 XOR gate implementations are plotted in Fig. 4. Notably, the gate with the maximum OPD ($OPD_{max} = 26.0\,\%$) achieves a relatively low CT ($CT = 27.76$ K), while the gate with the maximum CT ($CT_{max} = 132.70$ K) showcases an OPD below 10 %.

In summary, the exhaustive process of determining the best possible FoM values serves as a benchmark and reference point. It unveils, for the first time, the best FoM values that are generally attainable and provides insights into the scenarios where SiDB logic can be effectively employed. Furthermore, it yields several key findings: 1) For the first time, certain SiDB gates were found to operate at room temperature. 2) The number of utilized SiDBs emerges as a critical factor influencing the FoMs. 3) Individual gate implementations do not achieve the best possible values across all FoMs. Thus, the necessity of finding a trade-off becomes evident when aiming to optimize multiple FoMs simultaneously. This is investigated next.

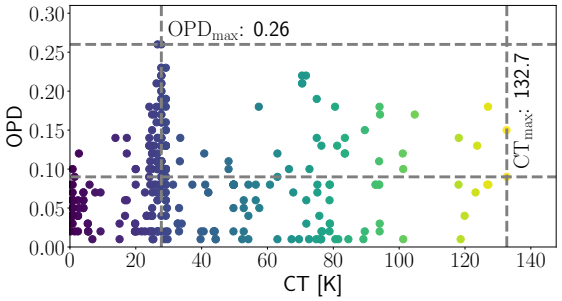


Fig. 4: OPD and CT values for all gates with $d = 4$ implementing XOR. CT values are represented using a color gradient: low CT values are shown in blue, while higher CT values transition through green to yellow.

TABLE II: FoM values for $\chi_{custom,min}$ with weights $w_i = 1$ across all 2-input Boolean functions. Results are sorted in ascending order of the cost value.

Gate	d	*CT* [K]	*OPD*	*MDC* [nm]		*BBR* [mV]	$\chi_{custom,min}$ ↗
				arsenic	vacancy		
NAND	4	400.00	0.37	4.78	6.09	27.48	**−1.77**
AND	4	102.3	0.16	3.88	6.17	23.35	**−1.49**
XOR	4	126.99	0.18	2.51	5.85	22.35	**−1.46**
NOR	4	400.00	0.03	3.70	9.43	26.67	**−1.26**
LE	5	400.00	0.03	3.69	9.43	26.67	**−1.26**
OR	4	115.54	0.24	3.78	3.84	23.79	**−1.15**
GE	4	400.00	0.03	6.62	6.84	25.78	**−1.05**
XNOR	5	80.35	0.13	4.92	5.81	27.04	**−1.04**
GT	5	107.40	0.13	3.85	6.19	23.63	**−0.95**
LT	4	60.83	0.46	4.28	7.08	22.13	**−0.76**

B. Finding a Trade-off to Minimize χ_{custom}

Given that the previously determined best possible FoM values cannot be simultaneously achieved by a single gate implementation, it becomes crucial to strike a balance between the individual FoMs when designing robust gates. In this section, gates are designed that offer the best trade-off

and thereby minimize χ_{custom}. To this end, Algorithm 1 is employed with the introduced cost function χ_{custom} with $w_i = 1$. The results are summarized in Table II. The gate names are listed in the first column, followed by the respective d and corresponding FoM values that minimize χ_{custom}. The minimal costs $\chi_{custom,min}$ are presented in the last column in ascending order.

a) $\chi_{custom,min}$ and Impact on Physical Design and Logic Synthesis: It is revealed that the minimum cost values $\chi_{custom,min}$ exhibit significant variability. For example, while the best gate implementation for the LT function exhibits the highest cost with $\chi_{custom,min} = -0.76$, the NAND function achieves a cost that is more than twice as low ($\chi_{custom,min} = -1.77$). The variation in cost provides valuable insights and opens up entirely new design approaches for circuits. These cost values can be utilized at higher abstraction levels, such as logic synthesis (technology mapping). One strategy involves steering clear of Boolean functions that exhibit high-cost gate implementations while favoring those with low-cost alternatives.

b) Number of Canvas SiDBs and FoM Trade-offs: Secondly, it is notable that the gates minimizing χ_{custom} neither comprise 2 nor 6 SiDBs. This observation aligns with expectations and the previous discussion, as the FoMs do not exhibit favorable values for these d. Moreover, the FoM values for the gate implementations minimizing χ_{custom} in Table II deviate significantly from the best possible values in Table I. However, the consistent deviation of all FoMs from their best possible values underscores the effectiveness of the implemented cost function and design approach to balance all FoM values. Therefore, it serves as a powerful tool, enabling the design of SiDB logic by effectively balancing the individual FoMs as required for the specific use case of SiDB logic.

VI. Conclusion

As the field of *Silicon Dangling Bond* (SiDB) logic advances and gains attention in both the academic and commercial communities as a promising beyond-CMOS technology, Figures of Merit (FoMs) to assess gate performance become crucial.

In this work, the following key objectives were addressed: 1) Introduction of a new FoM, called *Band Bending Resilience*. 2) Determination, presentation, and detailed discussion on the best achievable values for each FoM for all 2-input Boolean functions. 3) Presentation of the versatile cost function χ, unifying multiple FoMs tailored to specific application requirements and priorities. 4) Implementation of the optimization strategy using the cost function χ, which aims at designing SiDB logic with minimal cost, ensuring an optimal balance between all FoMs.

From the extensive determination of the FoM values, several key findings have emerged. Among the most important are: 1) SiDB logic is a promising beyond-CMOS technology on the absolute nanoscale since gates operating at room temperature could be designed for the first time, a feat previously predicted in the literature [29]. 2) The number of SiDBs used in gate design is a critical factor influencing the FoMs. 3) Achieving the best possible values across all FoMs is not feasible for individual gate implementations; rather, a trade-off must be determined. The cost function χ serves as a powerful method in this regard, as it integrates an arbitrary set of FoMs and can be readily extended to accommodate new FoMs in future endeavors.

To support open research and open data, the implementation and the simulation results are publicly available as part of the *Munich Nanotech Toolkit* (MNT, [28]).

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