ANCS
Architectures for Networking and Communications Systems

Monday, October 19

7:00 AM - 8:00 AM Breakfast and Registration

8:00 AM - 8:30 AM Welcome & Opening Remarks

8:30 AM - 9:30 AM Keynote

Software Radio: A Broad Change in RF Communications Systems Design

John Chapin, MIT & The Software Defined Radio Forum

Software radio is a deceptively simple idea: Identify all the features that specialize an RF communications device to a particular waveform (e.g. GSM cell phone or FM walkie talkie), and implement these features in flexible software on a generic platform, rather than in fixed-function hardware. This change should provide significant advantages compared to legacy hardware radios: the ability to support multiple waveforms on the same device, to upgrade the waveforms on the device through software downloads, and to dynamically adapt modulation or other physical layer parameters to a wide range of channel conditions. However, taking full advantage of software radio turns out to require a broad change in communications systems. Affected hardware components include antennas, filters, A/D converters, and power amplifiers. Affected device-level software components include signal processing, timing control, inter-layer APIs, and security. The hardware architectures optimal for this software are not GPPs, DSPs or FPGAs, but an interesting hybrid among these approaches. At the network level, new MAC algorithms and topology management are needed to exploit the flexibility of individual nodes. In this talk I present a slice through these varied and interrelated systems and research challenges, taking a total systems view of software radio.

Speaker Bio

John Chapin is a visiting scientist in the Claude E. Shannon Communication and Network Group at the Research Laboratory of Electronics of MIT. He spent 9 years in technical leadership roles at Vanu, Inc., a provider of SDR based cellular radio access networks. His work there on SDR and cognitive radio earned multiple awards including IEEE DYSPAN best paper, SDR Forum best paper, and SDR Forum Industry Achievement Award. Prior to Vanu he was on the faculty of the EECS department of MIT. He currently serves as chairman of the SDR Forum. He earned his Ph.D. degree in Computer Science from Stanford University in 1997.

9:30 AM - 10:00 AM Break

10:00 AM - 11:30 AM Programmable Platforms & Components

Cachecard: a Transparent Cache for Static and Dynamic Content on the NIC

Herbert Bos (Vrije Universiteit, The Netherlands); Kaiming Huang (Xiamen University, P.R. China)

Simplifying Data Path Processing in Next-Generation Routers

Qiang Wu (University of Massachusetts, USA); Danai Chasaki (University of Massachusetts, USA); Tilman Wolf (University of Massachusetts, USA) Exploitation and Threat Analysis of Open Mobile Devices Lei Liu (George Mason University, USA); Xinwen Zhang (Samsung Information Systems America, USA); Guanhua Yan (Los Alamos National Laboratory, USA); Songqing Chen (George Mason University, USA)

11:30 AM - 12:30 PM Lunch

12:30 PM - 2:00 PM Pattern Matching I

Evaluating Regular Expression Matching Engines on Network and General Purpose Processors

Michela Becchi (Washington University in St. Louis, USA); Charlie Wiseman (Washington University in St. Louis, USA); Patrick Crowley (Washington University in St. Louis, USA)

LaFA: Lookahead Finite Automata for Scalable Regular Expression Detection

Masanori Bando (Polytechnic Institute of NYU, USA); Nabi Sertac Artan (Polytechnic Institute of New York University, USA); H. Jonathan Chao (Polytechnic Institute of New York University, USA)

An Adaptive Hash-Based Multilayer Scheduler for L7-Filter on a Highly Threaded Hierarchical Multi-Core Server

Danhua Guo (University of California, Riverside, USA); Guangdeng Liao (University of California, Riverside, USA); Laxmi Bhuyan (University of California, USA); Bin Liu (Tsinghua University, P.R. China)

2:00 PM - 2:30 PM Poster Session 1

A NFA-Based Programmable Regular Expression Match Engine

Derek Pao (City University of Hong Kong, Hong Kong)

High Throughput Architecture for Packet Classification Using FPGA

Zhang Tao (University of Science and Technology of China, P.R. China); Wang Yonggang (University of Science and Technology of China, P.R. China); Zhang Lijun (University of Science and Technolgy of China, P.R. China); Yang Yang (University of Science and Technolgy of China, P.R. China)

A Block-Based Reservation Architecture for the Implementation of Large Packet Buffers

Hao Wang (University of California, San Diego, USA); Bill Lin (University of California, San Diego, USA)

OASis: Towards Extensible Open-Architecture Services Platforms

Yaxuan Qi (Tsinghua University, P.R. China); Fei He (Tsinghua University, P.R. China); Xiang Wang (University of Science and Technology of China, P.R. China); Chen Xinming (Tsinghua University, P.R. China); Yibo Xue (Tsinghua university, P.R. China); Jun Li (Tsinghua University, P.R. China)

EINIC: an Architecture for High Bandwidth Network I/O on Multi-Core Processors

Guangdeng Liao (University of California, Riverside, USA); Laxmi Bhuyan (University of California, USA); Danhua Guo (University of California, Riverside, USA); Steven R King (Intel Corporation, USA)

Accelerating Openflow Switching with Network Processors

Yan Luo (University of Massachusetts Lowell, USA); Pablo Cascón (University of Granada, Spain, Spain); Eric Murray (University of Massachusetts Lowell, USA); Julio Ortega Lopera (University of Granada, Spain)

Multiplexing Endpoints of HCA to Achieve Scalability for MPI Applications: Design, Implementation and Performance Evaluation with uDAPL

Jasjit Singh (Centre for Development of Advanced Computing, India); Yogeshwar Sonawane (Centre for Development of Advanced Computing, India)

Micro Secure Socket Layer (MSSL) for Micro Server

Hoa Nguyen (Keio University, Japan); Kensuke Naoe (Keio University, Japan); Yoshiyasu Takefuji (Keio University, Japan)

A Path Combinational Method for Multiple Pattern Matching

Tian Song (Beijing Institute of Technology, P.R. China); Dongsheng Wang (Tsinghua University, P.R. China)

A Lock-Free, Cache-Efficient Shared Ring Buffer for Multi-Core Architectures

Patrick Pak-Ching Lee (The Chinese University of Hong Kong, Hong Kong); Tian Bu (Bell labs, Lucent, USA); Girish Chandranmenon (Lucent Technologies, USA)

Hash-Based Routing for Scalable Datacenters

Mike Schlansker (HP Labs, USA); Jean Tourrilhes (HP Labs, USA); Yoshio Turner (HP Labs, USA); Jose Renato Santos (HP Labs, USA)

Theoretic Analysis of Finite Automata for Memory-Based Pattern Matching

Lucas Vespa (Southern Illinois University, USA); Ning Weng (Southern Illinois University at Carbondale, USA)

3:30 PM - 4:30 PM Performance Analysis

Design and Performance Analysis of a DRAM-Based Statistics Counter Array Architecture

Haiquan (Chuck) Zhao (Georgia Institute of Technology, USA); Hao Wang (University of California, San Diego, USA); Bill Lin (University of California, San Diego, USA); Jun Xu (Georgia Tech, USA)

Motivating Future Interconnects: A Differential Measurement Analysis of PCI Latency

David Miller (University of Cambridge, United Kingdom); Philip M Watts (University of Cambridge, United Kingdom); Andrew W. Moore (University of Cambridge, United Kingdom)

4:30 PM - 5:00 PM Break

5:00 PM - 6:30 PM Panel Session

Networking Hardware --What Drives Innovation?

Panel moderator: Jack Brassil, HP

Panelists:

Jonathan Smith, Prof., University of Pennsylvania

Flavio Bonomi, Distinguished Engineer, Cisco Systems

Keren Bergman, Prof., Columbia University

Paul Congdon, CTO, HP ProCurve

Ivan Seskar, Assoc. Director of IT, Winlab @ Rutgers University

Steve Muir, most recently CTO, Vanu Inc.

7:30 PM - 9:30 PM Dinner

ANCS
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Tuesday, October 20

7:30 AM - 8:30 AM Breakfast

8:30 AM - 9:30 AM Keynote

Revisiting the Internet Hourglass: Core Strength vs. Middle-Age Spread

Bruce Davie, Cisco

The threat of commoditization poses a real challenge for service providers. Offering only a "plain vanilla" IP packet delivery service limits the options for competitive differentiation. Conversely, embedding additional functionality in the network carries a number of risks -- decreased robustness and increased complexity, for example. The key to addressing this challenge is the careful selection of appropriate functionality to embed in the network. Functions should be added to the network only when they offer value to a wide range of applications, and they should not inhibit the correct operation of applications that do not need them. This talk addresses the question of how novel, useful functions might be embedded "inside" the network, and how best to evaluate candidate functions for inclusion.

For device designers, it is important to understand not only what functions are needed in the network today, but also which ones might provide the most benefit in the future. Because of the uncertainly about exactly what future networks will be expected to do, functions that are selected for inclusion in network devices must be as general as possible, and they should not interfere with the correct operation of the network when they are not needed. Some functions are best implemented as an overlay, leaving the essential network-layer functionality unaffected, while others will need assistance from the fast-path forwarding hardware. We will consider examples of various functions that have been or could be added to "core" networks, aiming to understand the tradeoffs both among different functions to add and among different implementation approaches.

Speaker Bio

Bruce Davie has worked in advanced development at Cisco Systems since 1995, and was awarded recognition as a Cisco Fellow in 1998. For many years he led the team of architects responsible for Multiprotocol Label Switching and IP Quality of Service. He recently joined the Video and Content Networking Business Unit in the Service Provider group. He has 20 years of networking and communications industry experience and has written numerous books, RFCs, and articles on networking. He is also an active participant in both the Internet Engineering Task Force and the Internet Research Task Force. Prior to joining Cisco he was director of internetworking research and chief scientist at Bell Communications Research. Bruce holds a Ph.D. in Computer Science from Edinburgh University and is a visiting lecturer at M.I.T. His research interests include routing, measurement, quality of service, transport protocols, and overlay networks.

9:30 AM - 10:00 AM Break

10:00 AM - 11:30 AM Interconnects

Weighted Random Oblivious Routing on Torus Networks

Rohit Sunkam Ramanujam (University of California, San Diego, USA); Bill Lin (University of California, San Diego, USA)

Design of a Scalable Nanophotonic Interconnect for Future Multicores

Avinash Kodi (Ohio University, USA); Randy Morris, Jr (Ohio Univeristy, USA)

A Novel 3D Layer-Multiplexed on-Chip Network

Rohit Sunkam Ramanujam (University of California, San Diego, USA); Bill Lin (University of California, San Diego, USA)

11:30 AM - 12:30 PM Lunch

12:30 PM - 2:00 PM High-Speed Lookup

Divide and Discriminate: Algorithm for Deterministic and Fast Hash Lookups

Domenico Ficara (University of Pisa, Italy); Stefano Giordano (University of Pisa, Italy); Sailesh Kumar (Huawei Technology, USA); Bill Lynch (Huawei Technology, USA)

Range Tries for Scalable Address Lookup

Ioannis Sourdis (Technical University of Delft, The Netherlands); Georgios Stefanakis (Technical University of Delft, The Netherlands); Ruben de Smet (Delft University of Technology, The Netherlands); Georgi Gaydadjiev (Technical University of Delft, The Netherlands)

Progressive Hashing for Packet Processing Using Set Associative Memory

Michel Hanna (University of Pittsburgh, USA); Socrates Demetriades (University of Pittsburgh, USA); Sangyeun Cho (University of Pittsburgh, USA); Rami Melhem (University of Pittsburgh, USA)

2:00 PM - 2:30 PM Poster Session

SPC-DFA: A Novel Technique for Multi-String Matching Acceleration

Junchen Jiang (Tsinghua University, P.R. China); Yi Tang (Tsinghua University,Beijing,China, P.R. China); Bin Liu (Tsinghua University, P.R. China); Yang Xu (Polytechnic Institute of New York University, USA); Xiaofei Wang (Dublin City University, P.R. China)

Memory Optimization for Packet Classification Algorithms

Viktor Pus (Brno University of Technology, Czech Republic); Jan Korenek (Brno University of Technology, Czech Republic); Juraj Blaho (Brno University of Technology, Czech Republic)

ISP Managed Peer-to-Peer

Shakir C James (Washington University in St. Louis, USA); Patrick Crowley (Washington University in St. Louis, USA)

Interfacing to a Virtualized Network Infrastructure Through Network Service Abstractions

Xin Huang (University of Massachusetts Amherst, USA); Shashank Shanbhag (University of Massachusetts, USA); Tilman Wolf (University of Massachusetts, USA)

Implementing URL-Based Forwarding on a Network Processor-Based Router Platform

Toshiro Yamauchi (Washington University in St.Louis, USA); Haowei Yuan (Washington University in St. Louis, USA); Patrick Crowley (Washington University in St. Louis, USA)

Parallelization of Snort on a Multi-Core Platform

Benjamin Y. Wun (Washington University, USA); Patrick Crowley (Washington University in St. Louis, USA); Arun Raghunath (Intel Corporation, USA)

Testbed for Evaluating Worm Containment Systems

Ritam Chakrovorty (Southern Illinois University, USA); Lucas Vespa (Southern Illinois University, USA); Ning Weng (Southern Illinois University at Carbondale, USA)

External Storage Middleware for Wireless Devices with Limited Resources

Mario A. Gomez-Rodriguez (CINVESTAV-Tamaulipas, Mexico); Victor J. Sosa-Sosa (CINVESTAV-Tamaulipas, Mexico); Ivan Lopez-Arevalo (CINVESTAV-Tamaulipas, Mexico)

Designing High-Speed Packet Processing Tasks At Arbitrary Levels of Abstraction - Implementation and Evaluation of a Mixmap System

Simon Hauger (University of Stuttgart, Germany)

SANS: A Scalable Architecture for Network Intrusion Prevention with Stateful Frontend

Fei He (Tsinghua University, P.R. China); Yaxuan Qi (Tsinghua University, P.R. China); Yibo Xue (Tsinghua university, P.R. China); Jun Li (Tsinghua University, P.R. China)

A Novel Hybrid SRAM/DRAM Memory Architecture for Fast Packet Buffers

Arthur Mutter (University of Stuttgart, Germany)

Binary Search on Levels Using a Bloom Filter for IPv6 Address Lookup

Kyuhee Lim (Ewha Womans University, Korea)

A Mobile Healthcare System Using IMS and the HL7 Framework

Stefanos Nikolidakis (University of Piraeus, Greece); Vasileios Giotsas (University of Piraeus, Greece); Dimitrios D. Vergados (University of Piraeus, Greece); Christos Douligeris (University of Piraeus, Greece)

3:30 PM - 5:00 PM Pattern Matching II

An Ultra High Throughput and Memory Efficient Pipeline Architecture for Multi-Match Packet Classification Without TCAMs

Yang Xu (Polytechnic Institute of New York University, USA); Zhaobo Liu (Polytechnic Institute of NYU, USA); Zhuoyuan Zhang (Polytechnic Institute of NYU, USA); H. Jonathan Chao (Polytechnic Institute of New York University, USA)

Co-Match: Fast and Efficient Packet Inspection for Multiple Flows

Chao Zhu (Institute of Computing Technology, Chinese Academy of Sciences, P.R. China); Mingshu Wang (Institute of Computing Technology, Chinese Academy of Sciences, P.R. China)

Experience with High-Speed Automated Application-Identification for Network-Management

Marco Canini (University of Genoa, Italy); Wei Li (University of Cambridge, United Kingdom); Martin Zadnik (CESNET, Czech Republic); Andrew W. Moore (University of Cambridge, United Kingdom)

5:00 PM - 5:30 PM Closing Remarks