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A Microelectronic Implementation of a Bioinspired Analog Matrix for Object Segmentation of a Visual Scene

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Abstract: In this paper we present a microelectronic implementation of a neural network of coupled oscillators that can segment black and white images. As an alternative to structures used in computer simulations where mathematical simplicity is more important, we used simple current mode astable multivibrators that can be easily implemented on silicon. Experimental results demonstrate the feasibility of this approach.

Introduction

It is well known that the visual system of higher animals and humans captures light from its surroundings through sensory cells of the retina. So, the representation of the outer world is made of discrete pixels at this level, one pixel for each sensory cell. However, Gestalt psychology demonstrates that humans perceive objects instead of discrete pixels. This means that some sort of processing should be done to transform these pixels into coherent objects, a process known as segmentation.

Some basic processing of the visual system is carried out in the retina [1] as detection of movement, filtering, etc. and then, information is led to the first layers of visual cortex where higher levels of perception, as scene segmentation, are placed.

It is obvious that some sort of segmentation must be done before perception of objects because there is too much redundant information in a raw matrix of pixels. However, to successfully segment an image, some knowledge of what is seen is also needed, so memory and attention are compulsive before segmentation. This suggests that there exists some kind of feedback between attention, memory and segmentation layers. This assumption is important when implementing a segmentation system because a successful process of perception as found in animals must be considered as a whole and not made of small pieces of different sub processes.

Experimental findings [2] [3] suggest that neural oscillations and phase locking of different populations of neurons of visual cortex are related to the perception of objects.

Some models have been developed to mimic that behaviour [4] [5] [6] [7] and some of them proved able to successfully segment real images. Among them, the LEGION algorithm is of high interest because of its good behaviour. However, implementing such an algorithm has the important drawback of the high computation load when compared to other standard segmentation algorithms [8]. The reason for such a big load is that a number of differential equations must be solved for every pixel, leading to a great number of mathematical operations for a simple image. This important drawback has led researchers to develop adaptations of this algorithm to speed it up [9]. However, this method is still computationally expensive.

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Hardware solutions have been proposed to solve this problem [10] [11] where instead of calculating the oscillator evolution, oscillators themselves are physically implemented in VLSI. However, a straight implementation of the equations proposed in software models may lead to area and power consuming designs. In this paper, we present the VLSI implementation and some results of a hardware model designed to reduce area and power consumption of the network [12].

Algorithm Overview

In this section, we give a quick overview to a segmentation algorithm developed by Wang and Terman [4] that has been successfully tested with different kind of images [9][13].
This algorithm, called LEGION (Locally Excitatory Globally Inhibitory Oscillator Network), consists of a 2-dimensional network of relaxation oscillators locally connected with positive coupling and a global cell negatively connected to all oscillators. Each oscillator is associated with a characteristic of the input scene (e.g. pixel intensity, motion, pre-processed acoustic components) (Fig. 1). When the segmentation process concludes, characteristics that belong to the same object are grouped together and oscillator phases code this binding information. For the sake of simplicity, simple luminance images with each pixel connected to one oscillator are used in this paper. Objects are groups of pixels of the same colour (black or white in this case) that are spatially connected to each other.

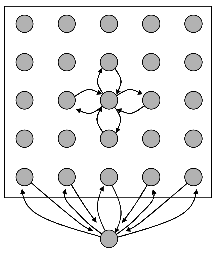

Figure 1: Network structure. Each circle represents a cell. Only excitatory centre cell connections and bottom line cell connections to inhibitor are shown for clarity.

The basic block of the LEGION network is the relaxation oscillator. The exact equation that gives the time behaviour of the oscillator is not important provided it has some basic properties [14]. Different equations have been used but the most common ones are given below:

$$\frac{dx_i}{dt} = 3x_i - x_i^3 + c - y_i + S_i + \rho$$
$$\frac{dy_i}{dt} = \varepsilon\left(\gamma\left(1 + \tanh\left(x_i / \beta\right)\right) - y_i\right) \qquad \text{Eq. 1}$$

Oscillator (i) is defined as a feedback loop between a fast excitatory unit (x_i) and a slow inhibitory unit (y_i). S_x represents excitatory and inhibitory synapses from nearest neighbours of oscillator i and from the global cell. ρ is the noise, a necessary term to apply a random component to the system strong enough to desynchronise oscillators that not belong to the same object. Obviously, this term should be included when simulating the equation system on a digital computer because digital operations only

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include very small truncating errors, however, it is not necessary in a physical analog implementation due to mismatch and real noise. Finally c, ε, γ and β are constants.
Excitatory synapses are positive couplings between adjacent cells. If two cells that are close enough and have a similar value (both are black or white in a b/w image or have similar luminance level in a monochrome image), an excitatory connection is established. When a cell goes active, that is to say, its ***x*** variable has a high value; its output synapses excite all cells that have an excitatory connection. On the other hand, when a cell is not in its active state (***x*** has a low value) synapse values are null.
Inhibitory synapses are negative couplings that are connected to all cells and their value depends on the state of a global cell or global inhibitor that reflects the state of the whole network. It activates when any cell of the network is active.

VLSI Friendly Algorithm

The basic oscillator we propose is an astable oscillator built of a damped integrator and a hysteresis comparator (Fig. 2).
Both oscillator subsystems can be analysed as integrators provided the comparator has a lower time constant than the integrator (Fig. 3).

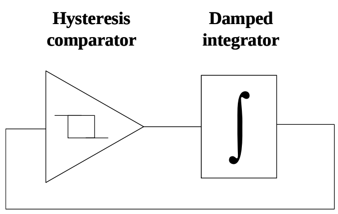

Figure 2: Block diagram of the basic oscillator

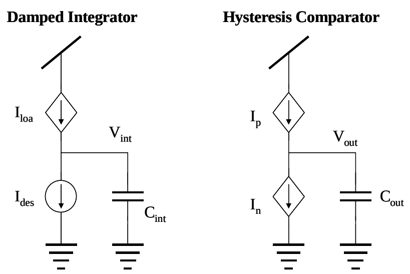

Figure 3: Simplified circuit diagram of the basic oscillator

The damped integrator consists of two current sources, namely I_{des}, which is constant and I_{loa}, which depends on the output voltage V_{out}. I_{loa} is zero when comparator output is low, thus capacitor C_{int} is progressively discharged. When comparator output is high, I_{loa} has a value higher than I_{des} hence capacitor C_{int} becomes charged.
The comparator is also an integrator, but much faster than the former. It implements a hysteresis cycle and creates a positive feedback. Current I_p has a small value when output voltage (V_{out}) is low therefore capacitor C_{out} is discharged. On the other hand, I_p has a higher value than I_n when output (V_{out}) is high thus charging capacitor C_{out}. I_n is a current that depends on the voltage of C_{int} with a monotonic growing function I_n=f(V_{int}).
Equations for this system are:

$$\begin{cases} \dfrac{dV_{out}}{dt} = \dfrac{I_p - I_n}{C_{out}}; & 0 < V_{out} < V_{\max} \\ \dfrac{dV_{out}}{dt} = 0; & other \\ \dfrac{dV_{\text{int}}}{dt} = \dfrac{I_{loa} - I_{des}}{C_{\text{int}}} \end{cases} \qquad \begin{cases} I_p = I_{pos}; & V_{out} < \vartheta_p \\ I_p = I_{wid} + I_{pos}; & V_{out} \geq \vartheta_p \\ I_{loa} = 0; & V_{out} < \vartheta_{loa} \\ I_{loa} = I_{loa0}; & V_{out} \geq \vartheta_{loa} \\ I_n = f(V_{\text{int}}) \end{cases} \qquad \text{Eq. 2}$$

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Where ϑ_{loa} and ϑ_p are thresholds, V_{max} is the power supply voltage, I_{des}, I_{loa0}, I_{pos} and I_{wid} are constants (I_{wid}+ I_{pos}>$I_n(V_{int})$> I_{pos} $\forall V_{int}$)
In addition to the basic behaviour, there is also synchronization between adjacent coupled cells. The mechanism we use to couple oscillators is a technique called Fast Threshold Modulation (FTM) [14]. It consists in shifting the state-plane orbit of the oscillator to force it to jump to the active state (V_{out}=V_{max}) when it is near enough to it.
Equation for I_p changes to I_p=I_{wid}+I_{pos}+I_{exc} when neighbour coupled cell is active and it does not change (I_p=I_{wid}+I_{pos}) when this cell is silent. I_{exc} is the excitatory current that shifts the oscillator orbit.
Note that two synchronized oscillators have different orbits than an oscillator with different or null excitation. To help synchronization, excitatory currents are normalised so the sum of all of them for a particular cell when all its neighbours are active is the same for each oscillator:

$$I_{exc,ij} = \frac{I_{exc}}{n}; \quad j = 1..n \qquad \text{Eq. 3}$$

where $I_{exc,ij}$ is the excitatory current contributed by coupled cell j to cell i and n is the number of coupled cells to i.
To desynchronise cells that do not belong to the same object, Selective Gating is used [4]. It consists in shifting all oscillator orbits in the opposite direction when any oscillator in the network is in its active state. That is to say, I_p= I_{pos}+[I_{wid}+ I_{exc}]-I_{inh} where I_{inh} is the inhibitory current. If an oscillator or any other oscillator of the same object is in its active state, I_{exc} will be bigger than I_{inh} and oscillations will not stop. On the other hand, if an oscillator is not in its active state, I_{inh} will be strong enough to prevent the oscillator to jump to its active state and delaying its oscillation. This segments oscillators that belong to different objects. It should be noted that if two oscillators are randomly synchronized, Selective Gating itself couldn't desynchronise them. To solve it, random noise must be added to digital simulations. However, experimental results presented in this paper show that it is not necessary to add this element when using analog hardware oscillators. Small mismatches between cells are strong enough to prevent random and power supply noise synchronization.

VLSI Implementation

In this section, we present the microelectronic implementation of the circuitry. As the most important application of such a design is to be used in very low power portable systems where digital computers may not be adequate, the main goal has been to reduce the area occupancy and power consumption and to maximize its possibilities to adjust parameters for testing purposes.
We have designed a 16x16 matrix of oscillators on a single chip using CMOS AMS 0.8 μm technology. The area occupancy of one cell (oscillator, complete synapses and one bit memory cell) without external wiring is 85x79μm^2. The full cell area is 129x90μm^2 and the total circuit area (including I/O PAD's) is 6.7mm^2. A microphotograph of the complete chip is shown in figure 5.
Communication to the exterior is a very delicate aspect of the circuit due to its parallel nature. In this experimental stage, an image should be loaded and the segmentation results have to be read by the external circuitry using a serial protocol to keep the number of I/O ports reasonable. However, the objective for practical uses should be to embed this network in an image sensor and/or in other parallel processing stages.

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To load the input image, we have chosen a single bit input that charges a 256-bit shift register. To output results, we use simple dynamic memory cells that can be read a row at a time. Therefore, information is stored in the internal memory and then read by the external circuitry by rows of 16 elements. This method of reading the network state at a precise time is used because the process can take more than a considerable fraction of oscillator cycle. Then, we can sample the whole network state at frequencies of the order of MHz that is fast enough to study its behaviour.

Experimental Results

To test the circuit we used a custom board to bias the analog circuitry and a PC with a digital data acquisition card to generate the digital sequences to input the image and output the results.

In figure 4, a successful segmentation is presented. After the left side image being loaded into the network, the state of the matrix of oscillators evolves through the four states on the right, and all three objects and the background are segmented.

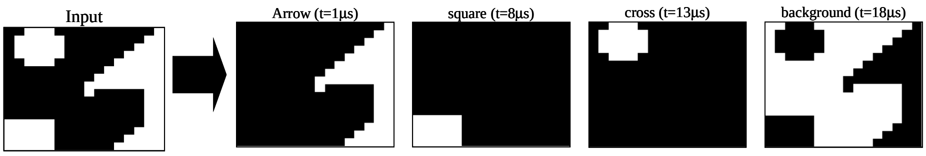

Figure 4: Input image and output at different time steps

Another application of this network is to count the number of objects in an image. As the global inhibitor goes high each time a group of pixels (object) activates, the frequency of the inhibitor is N times the frequency of any single oscillator in the network. The quotient of both frequencies is the number of objects in the scene. This result is presented in figure 6.

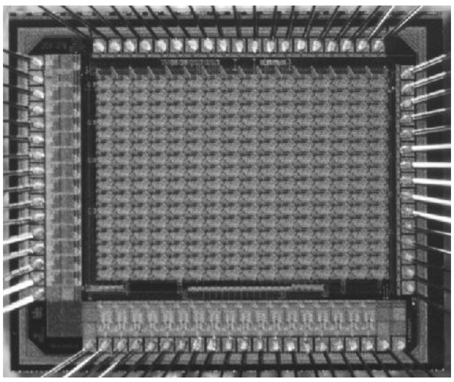

Figure 5: Microphotograph of the chip

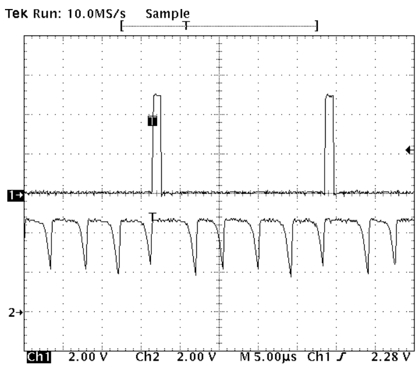

Figure 6: Time behaviour of one basic oscillator (top) and the inhibitor (bottom)

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Conclusions

In this paper, we have presented a microelectronic implementation of LEGION algorithm. To reduce power consumption and area occupancy we have used oscillators that are easily implemented in VLSI design without losing network functionality. Experimental results demonstrate the possibility of using the network to segment images faster than computer simulations and eventually it could be a reasonable alternative to traditional segmentation algorithms.
An important trade-off of this circuit is delays vs. power consumption. When biasing currents are too low (and also power consumption), delays between oscillators can be big enough to prevent oscillators from synchronizing, leading to inaccurate results. This figure is essential when comparing the oscillatory matrix with other methods, so, results that are more extensive and a comparison with other alternatives to segmentation, will be presented in following papers.

References

[1] M.Livingstone, D.Hubel: Segregation of Form, Color, Movement, and Depth: Anatomy, Physiology, and Perception. Science, 240, 740-749, (1988.)
[2] A.K.Engel, P.König, A.K.Kreiter, W.Singer: Interhemispheric Synchronization of Oscillatory Neuronal Responses in Cat Visual Cortex. Science, 252, 1177-1179, (1991)
[3] R.Eckhorn, R.Bauer, W.Jordan, M.Brosch, W.Kruse, M.Munk, H.J.Reitboeck: Coherent Oscillations: a Mechanism for Feature Linking in the Visual Cortex?, Biological Cybernetics, 60, 121-130, (1988).
[4] D.L.Wang, D.Terman: Image Segmentation Based on Oscillatory Correlation. Neural Computation, 9, 805-836, (1997).
[5] R. Eckhorn: Models of Visual Processing Derived from Cortical Microelectrode Recording. Biological and Artificial Computation. From Neuroscience to Technology, IWANN’97, 1005-1027, (1997).
[6] Z.Li: A Neural Model of Contour Integration in the Primary Visual Cortex. Neural Computation, 10, 903-940, (1998).
[7] Ch. Von der Malsburg, J.Buhman. Sensory Segmentation with Coupled Neural Networks. Biological Cybernetics, 67, 233-242, (1992).
[8] P.Baldi, R.Meir: Computing with Arrays of Coupled Oscillators: An Application to Preattentive Texture Discrimination. Neural Computation, 2, 458-471, (1990).
[9] Shareef, D.L.Wang, R.Yagel: Segmention of Medical Images Using LEGION. IEEE Transactions on Medical Imaging, 18, 74-91, (1999).
[10] J. Cosp, J.Madrenas, J.M.Moreno, J.Cabestany: Analog VLSI Implementation of a Relaxation Oscillator for Neuromorphic Networks. Neuromorphic Systems. Engineering Silicon from Neurobiology, 197-208, (1998).
[11] H.Ando, T.Morie, M.Nagata, A.Iwata: A Nonlinear Oscillator Network for Gray –level Image Segmentation and PWM/PPM Circuits for its VLSI Implementation. IEICE Trans, Fundamentals, E83-A, 2, 329-336, (2000).
[12] J.Cosp, J.Madrenas: A Neural Network for Scene Segmentation Based on Compact Astable Oscillators. 9th Int. Conf. on Artificial Neural Networks, 690-695, (1999).
[13] X.Liu, D.L.Wang: Range Image Segmentation Using a Relaxation Oscillator Network. IEEE Trans. On Neural Networks, 10, 564-573, (1999).
[14] D.Sommers, N.Kopell: Rapid Synchronization through Fast Threshold Modulation. Biological Cybernetics, 69, 393-407, (1995)