ESANN 2012 proceedings, European Symposium on Artificial Neural Networks, Computational Intelligence and Machine Learning. Bruges (Belgium), 25-27 April 2012, i6doc.com publ., ISBN 978-2-87419-049-0.
Available from http://www.i6doc.com/en/livre/?GCOI=28001100967420.

Towards biologically realistic multi-compartment neuron model emulation in analog VLSI

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Abstract. We present a new concept for multi-compartment emulation on neuromorphic hardware based on the BrainScaleS wafer-scale system. The implementation features complex dendrite routing capabilities, realistic scaling of compartmental parameters and active spike propagation. Simulations proof the circuit's capability of reproducing passive dendritic properties of a model from literature.

1 Introduction

Neuromorphic devices use CMOS hardware designed to imitate and understand structure and function of the brain to gain access to its computational power and efficiency. For this purpose, analog computing techniques are used to emulate differential equations of neurons using equivalent electronic circuits. A comprehensive review on neuromorphic circuits can be found in [1]. Depending on the application it is possible to choose parameters of these circuits to scale down the time constants of the differential equations to be much faster than real time. The dynamics are solved by analog emulation and not by digital computation. Hence, execution time does not scale with the number of components while power only scales linearly. Using VLSI[1] techniques allows to integrate hundreds of these components on a single chip to construct large networks. By interconnecting these chips, networks [2, 3] in the scale of millions of neurons are possible.

Most larger network simulations of biological neural networks are realized using single-compartment models, as computational complexity is much lower here. Thereby, complex dendritic structures are mapped onto a single point of equal potential, accepting the loss of dendritic computational power like local summing of synaptic input, or silent inhibition [4].

In multi-compartment modeling, dendrites are divided into sections of equal potential which are connected via conductances (see Fig. 1). Roughly simplified, the dendrite is treated as a discretized passive cable[5] without any active elements and with all synaptic input at the ends to simplify computation and to avoid handling of unknown channel density parameters on the dendrite [6]. Complex realistic multi-compartment simulations of cortical cells with active dendrites are presented in [7] for instance.

Few implementations of integrated analog multi-compartment neurons exist in literature. The key element is the resistor between the compartments as

[1] Very large scale integration

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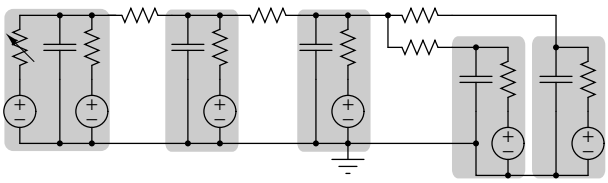

Fig. 1: Simplified schematic of a compartmental model with passive dendrites and one branching point.

adjustable resistors are hard to implement on a microchip if constraints like adjustability and small area consumption have to be met. Passive dendrites with switched capacitor resistor implementations have been studied in [8] and [9]. The work described in [10] uses current mode low pass filters and introduces active calcium channels. In [11] floating-gate transistors are applied to implement a resistive element between compartments; a 2 dimensional array could allow to map simple dendritic tree structures. In [12], a real-time VLSI multi-compartment neuron based on the circuits from [10] is used to observe the response of a dendritic compartment which is reduced to a sigmoid function.

Our implementation is based on the analog ASIC[2] HICANN[3] (see Fig. 2) of the BrainScaleS[4] Wafer-scale System (BWS) and is planned to be integrated into it. The BWS interconnects uncut silicon wafers with 200.000 adaptive exponential integrate-and-fire neurons (AdEx) [13, 14], to form networks in the range of millions of neurons. The emulation time is scaled down by a factor between 10^3 and 10^5 in comparison to biological real time.

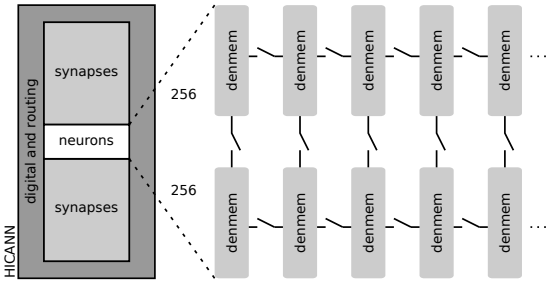

Fig. 2: Simplified schematic of the HICANN microchip, neuron configuration. 512 denmems arranged in two rows can be interconnected by switches.

A HICANN has two rows of 256 dendrite membrane circuits (denmem), each implementing the AdEx (see Fig. 2). A description can be found in [14]. Neurons are constructed by switching up to 64 denmems together by connecting their membranes and propagating their digital spike signal. This way the usage of

[2]Aplication-specific integrated circuit
[3]High Input Count Analog Neural Network
[4]www.BrainScaleS.eu

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routing resources can be optimized and the number of synapses (limited to 224 for a single denmem) can be enlarged to 14 336 per neuron. For a detailed description of this architecture see [15, 16].

2 Design concepts

Looking at the architecture of the HICANN described above, some parasitic multi compartment features, like a longitudinal resistance for interconnecting denmems already exist in the emulation. However, as the word parasitic suggests, these are not intended and cannot be controlled by the user. To transform this architecture to be capable of emulating biologically relevant spacial neurons, several steps have to be performed. The work presented in [17] has been chosen as reference for parameterization and dendritic morphology.

Each denmem can be a part of the soma or the dendrite now. Consequently, a very flexible parameterization is necessary because even models with small compartment numbers (e.g., eight) can have a dendritic compartment which is a factor 100 smaller than the somatic compartment (See eight compartment model of [17]). To manage these size factors, the parametrizability of the hardware neuron described in [14] has been enhanced by locally switching scaling factors of parameter biases for each single neuron, by introducing large additional capacitors for the soma and by dividing the capacitor of the neuron from [14] to enable a fine granularity for dendritic membrane capacitances. Furthermore, several denmems can be interconnected together to build one large soma compartment. Taken together, a factor of 100 between the size of somatic and dendritic compartments can easily be reached.

A major aspect of dendritic computation are active channels [18] in the dendrite generating dendritic spikes and back-propagating action potentials. They introduce a nonlinearity in each single compartment, hence simulation is more complex. In our hardware on the contrary, architecture, active channels are for free, as they are already implemented by the exponential term of the AdEx in each single compartment. To roughly emulate wide calcium action potentials [18, 17] we provide an individually adjustable current for pulling down the membrane to a reset voltage after a dendritic spike.

In the HICANN the undirected denmems are connected by switches (see Fig. 2) with a low but fixed resistance. Indeed, each compartmental denmen needs to have two connecting points now (Fig. 1) as there is one connection directed to the soma and one to the further dendritic tree. One of these connections can be equipped with a programmable resistor or switched to low resistance while the other one is only switched to save resources (Fig. 3). In the current implementation, the resistor can have values between 40 kΩ and 1.3 kΩ. It is implemented by transistors biased in ohmic region.

Each tail of a denmem is connected to a routing network enabling connections to its neighbours and its counterpart on the other side of the chip (Fig. 3). Furthermore it is possible to interconnect every four neurons. Sparsely, denmems with 6 units in between can be interconnected. The routing scheme allows to

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map the three dimensional dendrite structure onto the two level single dimension denmem arrangement. By realizing connections of every fourth neuron, the two rows of 256 denmems can be mapped onto two layers of 4 x 64 matrices. The architecture has been chosen to be capable of emulating at least the eight compartment model in [17] directly and with each compartment mapped to two hardware compartments.

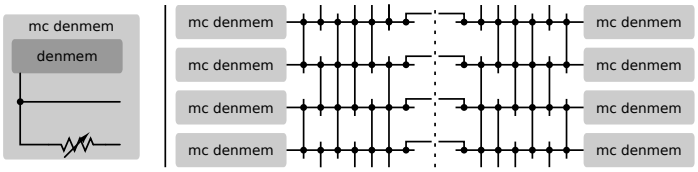

Fig. 3: denmem enhanced by resistive element (left) and dendrite routing scheme. Two switches are located at every connection dot connecting directly to the membrane or to the resistor.

3 Simulation Results

We reproduced results shown in [19]. The emulated neuron model is a four compartment model with one active somatic compartment and three equal passive dendritic compartments connected in a row by equal resistances. The model parameters can be found in [19]. To map the passive parameters of the model onto the hardware, membrane capacitors have been scaled down by a factor of 100 while conductances have multiplied by 500. This results in a scaling of the simulation time of 50 000. (compare time scales in Fig. 4)

The results can be found in Fig. 4 which is a copy of Fig. 4 B from [19] overlaid with the simulated membrane trace from the hardware model. The neuron is stimulated by a conductance pulse to a reversal potential (model) or a current pulse (our implementation) at the three different parts of the dendrite. The amplitude of the current pulse has been chosen to fit to the height of the first membrane trace. All other parameters have been directly calculated and mapped onto the hardware as described above.

4 Discussion and Outlook

The mapped hardware emulation fits well to the simulation. Nevertheless, the real circuit will be exposed to device variablity which can be counterbalanced by the individual parameterization of each compartment. A direct mapping like the one shown in Figure 4 will be possible after calibration of the circuit.

Our multi-compartment implementation will enhance the BWS by exploiting its given structure. The number of coupled differential equations is much larger for a multi-compartment model. Hence, the complexity of a computer simulation is larger and the speed and power gaining effect of neuromorphic hardware in comparison to simulators [14] is much more preeminent.

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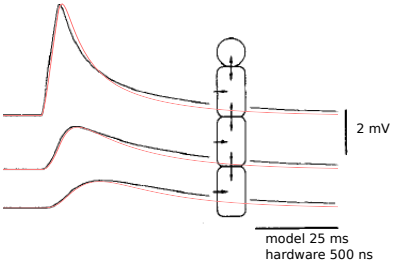
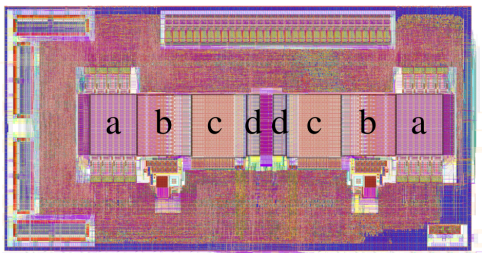


Fig. 4: Comparison between somatic membrane response to synaptic input at different parts of the dendrite in computer simulation (black) from [19] and a simulation of our hardware emulation (red)

The comparison of the passive properties has shown that it is possible to map a simple multi-compartment model, that has already been employed in literature [19], directly onto the hardware.

A test ASIC (see Fig. 5) is currently in production to proof the functionality of the new circuits. After in-silicon verification the multi-compartment neurons will be integrated into the HICANN chip and finally into the BWS.



specification	value
process	UMC 180 nm
denmems	64
synapses	1024
transistors	182 458
chip size	1.5 mm x 3 mm

Fig. 5: MCC mask layout (pads excluded) and chip specification. a: synapses, b: denmems, c: analog parameter storage, d: dendrite routing

Acknowledgements

The research leading to these results has received funding from the European Union 7th Framework Programme (FP7/2007-2013) under grant agreement no. 269921 (BrainScaleS)

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