Testing Technique of BIST: A Survey

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ABSTRACT
As the compactness of system-on-chip (SoC) increase, it becomes striking to integrate dedicated test logic on a chip. Starting with a broad idea of test problems, this survey paper focus on "Chip" Built in Self-Test (BIST) study and its promotion for board and system-level applications. This paper gives brief informative review of Built-in Self-test (BIST) and its testing techniques. Recently BIST Research is being highly used in VLSI and SoC testing for the detection fault coverage.

Keywords
Built-in Self-test, Circuit under test, Device under test, IC, SOC, CTL, PRNG, CRC.

1. INTRODUCTION
Built-in self-test (BIST) techniques constitute a group of techniques that provide the capability of performing high fault coverage with speed testing, whereas simultaneously they relax the reliance on expensive external testing tools. Hence, they constitute an attractive solution to the crisis of testing VLSI devices. BIST techniques are typically classified into online and offline. Offline architectures operate in either test mode or normal mode (during which the BIST circuitry is idle). During test mode, the inputs generated by a test generator unit are applied to the inputs of the circuit under test (CUT) and the results are captured into a response verifier (RV). Consequently, to perform the test, the normal operation of the circuit under test is stalled and, therefore, the performance of the system in which the circuit is included, is degraded. The functionality of gadgets and electronics equipment's has achieved a phenomenal growth over the last two decades while their physical sizes have come down significantly. The main reason is, due to the rapid advances in IC technologies, which enables fabrication of several millions of transistors in a single chip or integrated circuit (IC). According to Moore's law, number of transistors in a chip doubles in every 1.5 years. With the recent research in the technology, device shrinks to nanometer scale, but complexity and density of the chips keep on increasing. This may result in device failure and many manufacturing faults. Reduction in the feature sizes results in growing the fault detection and manufacturing faults becomes very difficult. VLSI testing is becoming more and more important and challenging to verify a device functions are properly or not. Conventional automatic test equipment (ATE) based testing technique is no longer able to handle the rising test challenges. The built-in self-test (BIST) is widely used in the online testing while chip in normal operation. In case of offline BIST chip is not in normal operation. The requirement of efficient and economical testing method such as the Built-In Self-Test (BIST) increases with the increase in complexity of Very Large Scale Integration (VLSI) devices or System-on-Chip (SoC) [2]. The logic behind BIST is to design an IC that is capable of verifying itself as being either fault-free or faulty and then continue its operation when the testing is not being carried out.

2. BACKGROUND AND MOTIVATION OF RESEARCH
The Built-in Self-test (BIST) concept originated with the idea of including a pseudorandom number generator (PRNG) and cyclic redundancy check (CRC) on the chip. If all the registers that hold state in an chip are on several internal scan chains, then the task of the registers and the combinational logic between them will generate a unique CRC signature over a large enough test of random inputs. So all a chip need do is store the expected CRC signature and test for it after a large enough sample set from the pseudorandom number generator.

2.1 BIST (Built-in Self-test)
BIST Places the job of device testing inside the device itself and generates its own stimulus and analyzes its own response. The trend to include more test logic on an ASIC has already been mentioned. Built-in self-test (BIST) is a set of structured-test techniques for combinational and sequential logic, memories, multipliers, and other embedded logic blocks. In each case the principle is to generate test vectors, apply them to the device under test (DUT) or circuit under test (CUT), and then verify the response. The architecture of BIST technique is shown below which having three main components are CUT, TPG, and ORA[1].

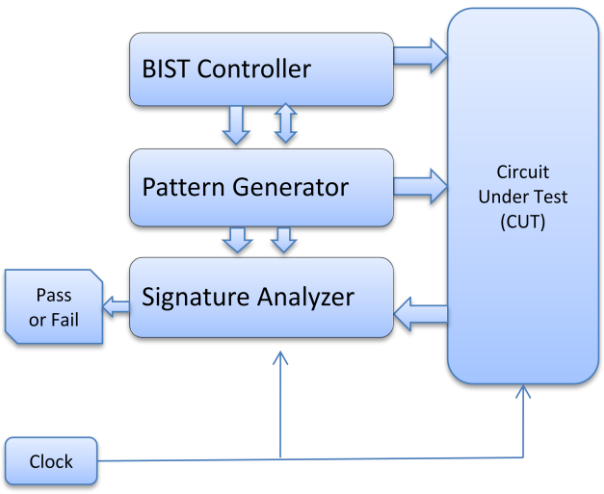

Fig 1. Architecture of BIST technique[1]

3. LITERATURE SURVEY
In the earlier period, several researchers and authors have investigated the BIST testing techniques for the detection of fault coverage. In this survey paper various related literature such as IEEE transactions, other journals and proceedings of various national and international conferences were reviewed.

S Sivanantham, et. al.[2] Proposed an Adaptive Low Power RTPG for BIST based test applications. In this research paper, researcher concerned about the power reduction during testing

in scan based tests. But methods to reduce shift power will results in test coverage loss. So Low Power Random Test Pattern Generator (LPRTPG) is presenting to get better the tradeoff between shift power reduction and the test coverage loss. For getting the required tradeoff, an adaptive type performance is utilizing where the previous test results are given as feedback to a transition controller which is proficient of generating highly correlated test patterns. The tentative results on ISCAS'89 benchmark circuits' shows effectiveness of the work in terms of reduction in test power.

Ioannis Voyiatzis et.al.[3] Proposed an Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells. In this research paper, Input vector monitoring concurrent built-in self test (BIST) technique perform testing during the normal operation of the circuit without imposing a require to set the circuit offline to perform the test. These techniques are evaluated based on the hardware overhead and the concurrent test latency (CTL), whereas the circuit operates normally. In this brief discussion, researcher presents a novel input vector monitoring concurrent BIST technique, which is based on the scheme of monitoring a set of vectors reaching the circuit inputs during normal operation, and the use of a static-RAM like structure to store the comparative locations of the vectors that attain the circuit inputs in the examined window.

D. C. Huang et. al.[4] Discussed about An Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers. In this paper, researchers proposed a new transparent built-in self-test (T-BIST) technique to test multiple embedded memory arrays with various sizes in parallel. Also a new transparent test interface is designed to perform testing in the normal mode and to cope with nested interrupts in a real-time manner is discussed. They also developed a very powerful signature analysis technique to eliminate the tedious signature prediction process with almost no hardware cost. Based on the memory background data, an efficient TRSMarch algorithm, March algorithm, has also been developed to generate test patterns and expected test results.

Bernard Courtois et. al. [5] Proposed an On-Line and OFF-Line testing from digital to analog, from circuits to Board. The main goal of this research paper is to survey the design of circuit and system featuring testing capabilities. Design of failsafe reliable of Circuit Board and ASICs is broadly addressed.

Petr Fiser et.al. [6] Proposed a Survey of the Algorithms in the Column-Matching BIST Technique. A discussion on possible heuristic algorithms solving the major part of BIST synthesis method, the Column Matching. The main part of this research paper is BIST design is an output decoder transforming pseudo-random LFSR code words into deterministic tests pre-computed by an ATPG instrument.

Jahangiri et.al.[7] have tried to examine test patterns for IC's that are both secure and have very high exposure. Protected applications often require high test quality with rising demands at 65 nanometer and below. A test method that is protected is necessary such that the test can be conducted outside of a costly protected test environment. Logic BIST is the most protected test method. However, for some devices, it doesn't provide a high enough test support or quality recently desired fault models.

Jinkyu Lee et.al.[8] Proposed LFSR Reseeding Scheme Achieving Low-Power dissipation during Test. several test data compression schemes are based on LFSR reseeding. A disadvantage of these techniques is that the unspecified bits are contain random values resulting in a large number of transitions during scan-in, as a result causing high power dissipation. This article presents a new encoding technique that can be used in conjunction with any LFSR reseeding scheme to significantly reduce test power and even further decrease test storage. The proposed encoding technique acts as a second stage of compression after LFSR reseeding. There are two goals which are: First, it decreases the number of transitions in the scan chains and second it reduces the number of bits that need to be generated via LFSR reseeding algorithm. An experimental result shows that the proposed scheme significantly reduces test power and in several cases provides greater test data compression than LFSR reseeding technique.

G. Sudhagar et.al.[9] Discussed about the novel architecture for vlsi design. The time, power, and data volume are among some of the most challenging issues for testing IC's and have not been fully determined, but also scan-based scheme is used. A novel architecture, referred to the Selective Trigger-Scan architecture, introduced in this article to address these issues. This architecture reduces switching action in the circuit-under-test (CUT) and increases the clock frequency of the scanning process. A secondary chain is utilized in this architecture to avoid the large number of transitions to the CUT during the scan in process, also enabling retention of the currently applied test vectors and applying only essential changes to them. It also allows delay fault testing. Using ISCAS-85 and ISCAS-89 benchmark circuits, the efficiency of this architecture for improving SoC. These test such as, time, and data volume is experimentally evaluated and confirmed.

Xijiang Lin et.al.[10] proposed an Adaptive Low Shift Power Test Pattern Generator for Logic-BIST. While increasing the correlation between adjacent test stimulus bits can significantly decrease shift power consumption. Though, it often causes test coverage loss when applying it to decrease the shift power consumption in logic Built-in Self-test. In this article, a new adaptive low shift power random test pattern generator (ALP-RTPG) is presented to get better the tradeoff among test coverage loss and shift power reduction in logic-BIST.

This is achieved by applying the information derived from test responses to dynamically adjust the correlation between adjacent test stimulus bits. When comparing with an available method, called LT-RTPG, experimental results for industrial designs show that the projected method can significantly decrease the test coverage loss while still achieving dramatic shift power reduction.

Rinitha.R et.al. [11] Discussed about Built in self-test and provide brief information about its test application. As the compactness of system-on-chip increase, it becomes striking to integrate dedicated test logic on a chip. In this survey test applications and its terms, common test methods and analyze the basic test procedure are mainly focused. The concept of Built-in Self-Test (BIST) is introduced and discussed. This BIST technique not only offers economic profit but also provides attractive technical opportunities with respect to hierarchical testing and the reprocess of test logic during the application of the VLSI circuit. Recently BIST Research is being highly used in receiver system and wireless transmitter for the detection of mismatch and non-linear parameters.

After brief analysis of Journals and articles, we have listed out some advantages and disadvantages mentioned in the table 1 below.

Table 1. Literature comparison and there advantages and disadvantages

Author	Proposed Technique	Advantage	Disadvantage
Renju Thomas John	Adaptive Low Power RTPG for BIST	power reduct ion during testing	reduce shift power will results in test coverage loss,
Ioannis Voyiatzis	Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells	The proposed method is shown to be more efficient than previously proposed input vector monitoring concurrent BIST techniques in terms of hardware overhead and CTL	Hardware overhead and CTL trade-off, Complexity.
D. C. Huang	Efficient Parallel Transparent BIST Method for Multiple Embedded Memory Buffers	reduce the hardware overhead without losing fault coverage	More Complexity and High power requirement
Jinkyu Lee	LFSR Reseeding Scheme Achieving Low-Power dissipation during Test	Reduce test power and even further decrease test storage.	BITS are contain random values resulting in a large number of transitions during scan-in.
G. Sudhagar	Novel architecture for VLSI testing	Reduces switching action in the circuit-under-test (CUT) and increases the clock frequency of the scanning process	delay fault testing and Higher Cost.

4. BIST TECHNIQUES

After analysis of various journals and articles, it can be conclude that, there are two main techniques are used in Built-in Self-test (BIST) is On-Line BIST and Off-Line BIST but we also found some BIST testing techniques are shown below in table 2. with their fault coverage and study directions[12][7].

Table 2. BIST Techniques

BIST TECHNIQUE	FAULT COVERAGE	STUDY DIRECTIONS
Internal MBIST	IC internal defects: dynamic fault, stuck at fault	Algorithms
External MBIST	External memory Defects: RLDRAM, FCRAM, DDR, TCAM, SSRAM stuck at fault, dynamic fault. Interconnect defects: process defect SOQ/ PCOLA and SSN	Algorithms , Diagnosis
Logic BIST	IC internal defects	Applications , resolve NTFs issues
High speed IO BIST	Interconnect defect - SI /noise defects.	Algorithms , interconnect between different vendors ICs, interconnect over backplanes
Frame BIST	IC internal defects, process defect, and system-level malfunctions	Instruments - - Protocol based pattern generation, Algorithms, diagnosis
On chip instruments	IC internal defects, board and Interconnect defects. Process defects	Algorithms , interconnect between different vendors ICs, interconnect over backplanes, voltage and temperature measure
Analog and mixed signal BIST	IC internal defects, and Interconnect defects	Algorithms , Diagnosis

5. CONCLUSION

Technologies are changing at fast pace. BIST is a testing technique used for finding faults in integrated circuits (ICs), which consist of many BIST testing techniques proposed by different authors and researchers. After exhaustive literature survey show in the above section all state of art methods and ideas where discussed and analyze that OFF-Line BIST is the only testing technique, which is used to test VLSI circuits or IC's during normal operation. It is not enough to distinguish between different techniques, hints paper has shown difference between various techniques based on different parameters. Paper will guide new researchers to fetch clear information about BIST through a single paper. After comparison of many journals and articles we formulated that On-Line BIST and Off-Line BIST testing scheme is mostly used in the industries for testing of VLSI circuits and IC's.

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