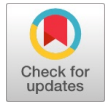# A Systematic Journal of Multipliers Accuracy and Performance

E. Jagadeeswara Rao, Durgesh Nandan, R.V. Vijaya Krishna, K. Jayaram Kumar

Abstract: Low power and efficient architecture of computer arithmetic is demanded of real time Digital signal processing. Out of all arithmetic units, the multiplier is most important and frequently used arithmetic component in literature. As we know that there are many multipliers exist in the literature and everyone has his own proc-corns. But there is a gap in literature, no one gets compared all popular multiplier technique at same platform and discuss their advantages and limitations at one place. This research work outlines the most popular five multiplier techniques (like Wallace, modified, Vedic, Russian Peasant and Logarithm) and compares them, highlights merits, demerit for further improvements. This comprehensive study includes the systematic development, compares the latest design of every multiplier and justified that which one is better over other reported multiplier is also highlighted.

Keywords: Wallace multiplier, Modified both multiplier, Vedic multiplier, Russian peasant multiplier Logarithm multiplier.

I. INTRODUCTION

Multiplication is main component in arithmetic circuits. It is used frequently in Digital signal processing (DSP), Image processors and neural network. Every DSP and image processors consist of multiplication functions like multiply, accumulate, Multiplier-accumulator (MAC) convolution and filtering. In DSP algorithms multiplication takes around 80 % of total execution time compared to other operations. So, Multiplier performance decides the overall performance of DSP algorithm performance.

In this research work, we only focus on the various types of the multiplier designs for performing comparative analysis about hardware performance and accuracy concerns. Not only that, we try to found the most suitable multiplier for the various type of DSP applications and Image Processing applications [1], [2], [3]. The comparative performance comparison was done among the most popular five multiplier techniques (like Wallace, Modified, Vedic, Russian Peasant and Logarithm). Rest of research paper is rearranged as follows: Reported literature has been explored further in Section 2. Section 3 explores the comparison of

results. Finally, the finding of the multiplier design is concluded in Section 4.

II. SYSTEMATIC LITERATURE

As we discuss earlier, there is 1000 of multiplier in literature but no one is perfect. Everyone has is own proc-corns. For accuracy and performance analysis of multiplier, 5 most popular multiplier get chosen and discussed in this research paper. These are Wallace Multiplier (WM), Modified Both Multiplier (MBM), Vedic Multiplier (VM), Russian Peasant Multiplier (RPM) and Logarithm Multiplier (LM). One by one, we have discussed systematic development of each multiplier.

A. Wallace Multiplier

At 1964, C. S. Wallace has proposed the new fast multiplier scheme Known as WM based on the sequential adding stages reduction by reducing the Partial Product (PP) accumulation [4]. In 1998, M. E. Robinson and E. Swartzlander Junior has proposed WM by using 4:3 counters for optimizing the hardware performance and found up to 10% less delay [5]. In 2010, Ron S. Waters and E. Swartzlander Junior has modified the conventional WM with a nearly same delay [6]. In 2011, S. Rajaram and K. Vanithamani has proposed a WM which reduce the delays [7], [8], [9]. The modified WM reduces 80% of HAs [10].

Fast column compression techniques in multiplication have been acquired by using combination of two different designs. The results demonstrated that fast column compression multiplier is 41.1% faster than the 64-bit regular WM [11]. 8-Bit hybrid tree multiplier is developed by combining Wallace and Dadda methods and found 40% of power reduction [12]. The modifications of Wallace/Dadda multiplier use carry-look-ahead adders as a replacement of full adders [13], [14]. In 2018, E. Jagadeeswara Rao (2018) proposed high speed WM [15]. In this design a high-speed adder with 4-2 and 8-2 adder compressor was used at reduction stage and increases speed 25% in comparison of reported WMs [15].

B. Modified Booth Multiplier

In 1950, Booth Donald has proposed new algorithm for multiplying two unsigned (or signed) numbers which is known as Booth multiplier [16]. In 2000, Chang Yeh and Chein Wei Jen has proposed a new modified Booth Encoding Scheme (MES) [17]. It increases 25% speed in comparison of conventional MBM [17]. In same year 2000, Fayez Elguibaly has proposed MBM with parallel MAC unit [18]. It was three times faster than the standard MAC unit. In 2007, Zhou Shun *et al.* has proposed a radix-4 MBM with

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multi precision reconfigurable scheme which can be cascaded to comply with the different input length [19]. In 2010, S. R. Kuang and J. P. Wang has proposed low power configurable MBM [20]. But it had extra overhead circuit, it has hardware overhead in comparisons of the regular multipliers but their power consumption is significantly reduced. In 2012, R. P. Rajput and M. N. S. Swamy has proposed a high speed MBM which uses CSA and CLA [21]. In 2014, Kostas Tsoumanis *et al.* has proposed MBM with Fused Add Multiply (FAM) [22]. In 2016, K. Tsoumanis and N. Axelos has developed a new MBM hardware with pre-encoded scheme, in which reduce the area at encoding stage also reduce delay and power consumption [23]. In 2017, W. Liu and C. Wang has designed a new approximate radix-4 MBM in which reduce the power and delay [24]. Also designed new two approximate PP generation circuits and reduce the area at this level compare to existing PP generation circuit.

C. Vedic Multiplier

In 2009, P. Mehta and D. Gawali has first time to compare the traditional multiplier and VM based on Urdhva Tiryakbham and give the same hardware expense [25]. In 2012, Kanchigi *et al.* has designed a VM architecture with pipelined technique [26]. It performs with high speed and low power compare to traditional WM and MBM. In 2013, Pavan Kumar U.C.S *et al* designed a VM based on Nikhilam sutra using barrel shifter with reduced 45% delay [27].

In 2014, R. Anjana. *et al.* has designed a VM with kogge stone adder with 25% enhanced speed [28], [29]. In 2014, Hardic Sangani *et al.* has proposed VM based on Differential Cascade Pre-resolve Adiabatic Logic (DCPAL) with reduced 57% power [30]. In 2016, K. D. Rao *et al.* has proposed VM based on the URDHVA TIRYAKBHYAM sutra and an N×N Vedic real multiplier with minimum path delay architecture is developed [31]. In 2017, R. Katreepalli and T. Haniotakis has (2017) proposed an efficient design of VM using Manchester Carry Chain (MCC) adder in a hierarchal approach [32]. In 2018, S. Sharma and Vangmayee has designed VM using Gate Diffusion Insulator (GDI) with reduced power and area [33].

D. Russian Peasant Multiplier

In 2014, K. Gunasekaran and M. Manikandan has proposed a new multiplier architecture is called Russian peasant multiplier by using CSA [34]. It increases 25% speed in comparison of traditional VM. In same year with same author combination has designed the RPM with sklansky adder with reduced area and delay compare in comparison of RPM [35]. In 2016, C. Uthaya Kumar and B. Justus Rabi has proposed a RPM with Modified Square Root Carry Select Adder (MSRCSA) with improvement of 18.32 % power consumption compare to conventional RPM [36]. In 2017, N. C. Sendhikumar has designed the RPM by using RCA with improvement of 10.45 % delay compare to existing RPM [37]. In 2018, E. Jagadeeswara Rao and A. Rama Vasantha has designed approximate RPM with high speed adder compressor in which adder compressor designed with 8-2 adder compressor. It also reduces 25% delay compare to traditional RPM [38].

E. Logarithm Multiplier

In 1962, J.N. Mitchell was suggested an algorithm which is based on add-and-shift operation for the logarithm multiplication and logarithm division [39]. In 1975, Swartzlander *et al.* have suggested the sign logarithm number system [40]. It was fast algorithms for performing basic arithmetic operations. In 1999, SanGregory's has proposed correcting algorithm [41]. That was was simple and fast in operation because it uses only mantissa's four Most Significant Bit (MSB) for adjustment. In 2006, V. Mahalingam *et.al* has suggested the Operand Decomposition (OD) [42]. It is as an independent approach to minimize the error and has applied to all previous logarithmic multiplication approaches. During 2010 to 2013, the iterative logarithmic approximation was introduced which was based on the correction terms with the high-level of parallelism [43], [44]. In 2016-2018, Durgesh Nandan *et al.* has suggested various changes in logarithm multiplier to make it best in comparisons of existing design [45], [46], [47], [48], [49], [50], [51], [52].

III. RESULTS

For proper understanding and performance analysis of existing most 5 popular multipliers, we study the all latest design of WM, MBM, VM, RPM and LM.

Table 1: Hardware performance comparison of various multipliers

Design	Area (Slices/LUTs)	Delay(ns)	Errors (%)
WM [4]	93 Slices/182 LUTs	31.469	--
WM [7]	79 Slices/142 LUTs	16.556	--
WM [11]	77 Slices/112 LUTs	23.587	--
WM [12]	59 Slices/113 LUTs	19.662	--
WM [13]	52 Slices/99 LUTs	14.329	--
WM [14]	45 Slices/88 LUTs	15.784	--
WM [15]	41 Slices/79 LUTs	9.033	--
MBM [16]	65 Slices/105 LUTs	14.567	--
MBM [21]	59 Slices/101 LUTs	10.551	--
MBM [22]	68 Slices/110 LUTs	9.257	--
MBM [23]	69 Slices/106 LUTs	11.728	--
MBM [24]	63 Slices/102 LUTs	12.827	--
VM [25]	101 Slices/199 LUTs	31.869	--
VM [26]	106 Slices/195 LUTs	25.646	--

VM [27]	104 Slices/189 LUTs	23.355	--
VM [28]	99 Slices/178 LUTs	22.556	--
VM [30]	102 Slices/185 LUTs	34.674	--
VM [31]	93 Slices/175 LUTs	22.551	--
VM [32]	85 Slices/165 LUTs	21.257	--
VM [33]	87 Slices/159 LUTs	33.877	--
RPM [34]	95 Slices/186 LUTs	31.469	--
RPM [35]	89 Slices/165 LUTs	19.646	--
RPM [36]	91 Slices/160 LUTs	21.355	--
RPM [37]	79 Slices/142 LUTs	16.556	--
RPM [38]	64 Slices/114 LUTs	12.674	--
LM [39]	217 Slices/20 LUTs	8.384	3.77
LM [42]	271 Slices	13.868	1.449
LM [48]	65 Slices	10.025	1.678

All latest architecture design of multipliers has been simulated by using Xilinx 14.7. Analysis has been done in terms of accuracy as well as hardware complexity. Results are implemented and applied with the same 8-bit input patterns for fair error analysis, which is shown in Table 1.

IV. CONCLUSION

Till now, many authors try to concluded various design of multiplier and which one is best multiplier till ever at literature but they were partial concluded. In this paper we discuss about the multipliers, systematic development in field of multiplier and which one is best in what condition. This comprehensive study includes the techniques used by researchers to improve the design of multiplication. Based on this analysis conclude that the logarithmic multiplier is the best choice for designers if accuracy is not main concern. But the Wallace multiplier is the most efficient design in terms of area, speed, latency, accuracy. However, if logarithm multiplier is implemented by logarithm converter and antilogarithm converter with advanced correction circuit, it must become the most efficient design with best performance. This enhancement is hoped to contribute significant improvements in digital signal processing systems and image processing area.

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