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Reduction of Power in General Purpose Processor Through Clock-Gating Technique

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Abstract: ***Now a days DC power supply plays very important role in the Electronic industry because for every electronic gadget DC power is required to operate it. Even though durable DC batteries are available in the market to operate the various electronic gadgets for more time, electronic designers are continuously concentrating more and more to reduce the power through the various new Technologies like increasing parallel operations, pipe line concepts [1] etc. To work such durable batteries more duration than the actual duration what they can give, in this work we are concentrating on the 'clock-gating' technique to reduce the power in the general purpose microprocessor. For every microprocessor clock is required. All operations of any processor are performed by the clock cycle. There are various blocks in the processor but all the blocks are not operated at a time while using it, some blocks in the off mode while other blocks are in the working mode. Hence in order to power off such blocks for a little while clock gating is used in this work. Wherever particular block is not operated, for that block clock is disabled by the clock gating technique. The main principle of clock getting is nothing but ANDing the processor clock with a gate-control signal.***

Keywords: ***DC Power, Electronic Gadgets, Clock Gating, General Purpose Microprocessor, Clock Cycle.***

I. INTRODUCTION

Without the power, no system is operated in the nature. Power is two types, AC power and DC power. AC power is used for all the electrical applications whereas DC power is used for all electronic applications. DC power is generated by converting AC to DC adaptors but we cannot carry easily such setup from one place to other place. Hence, portable batteries like Lithium, Cadmium DC batteries came into the picture. Such portable DC batteries may give more durability.

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But to extend the DC battery run time further, researchers are concentrating on the more design optimization techniques. If we optimize the design of electronic devices then the power consumption will be reduced hence battery run time will be increased more than normal [2].

For the past few years power sensitive devices have got the more importance because all the portable electronic appliances are being used portable power supplies like lithium, cadmium batteries. Examples of such electronic appliances are cell phones, personal digital assistants, notebook, laptop, palmtop and portable communication devices.

For every 'technology generation' power consumption is increased due to the increased frequencies and increased density of transistors in the die. But upto certain limits scaling of supply voltage is maintained the power consumption. For high performance applications scaling of voltages have certain limits [3]. Hence to maintain the power density within limits only voltage scaling is not sufficient hence it leads to power sensitive applications.

Dissipation of power by the circuits of VLSI:

There are two types of power dissipations or consumptions by the VLSI circuits i.e., static power dissipation and dynamic power dissipation.

Static power consumption:

Any VLSI circuit is the combination of combinational logic circuits and sequential logic circuits. Such combinational and sequential logic circuits are designed by logic gates.

Logic gates will consume the power in two ways that is first one is static power consumption and second one is dynamic power consumption. When the static current flows from V_{DD} to V_{SS} or supply rails then that current multiplied by resistance is called static resistance. Consumption of static power is occurred in NMOS technology because in NMOS technology pull up transistor is depletion mode transistor which should act as always ON resistance. Hence, static current will flow from V_{DD} to V_{SS} when pull down transistor is on. When such static current multiplied by ON resistance of pull up and pull down transistors then it gives rise to static power of that particular logic circuit. Apart from this type of static power dissipation, at the transistor level in the nano meter range there are some other leakage powers which cannot be avoided. In NMOS FET or PMOS FET these are –

1. Leakage power due to reverse biased PN junction at drain and substrate terminals. 2. Gate terminal leakage current due to direct tunneling between potential barrier and SiO_2 layer. 3. Leakage current due to sub-threshold.

Dynamic power consumption:

Dynamic power consumption occurs when ON and OFF switching actions take place for the pull up and pull down transistors for a given VLSI circuits. When the load capacitance is being charged or discharged, depending on operation of the logic circuit this dynamic power is produced.

We can observe dynamic power consumption in all CMOS circuits because in CMOS circuits pull up is PMOS transistors and pull-down is NMOS transistors. When input voltage logic '0' is applied pull up transistor comes to ON position and hence the load capacitance C_L is charged, at that time pull down transistor is in OFF condition. Similarly, when input voltage logic 1 is applied pull down transistor comes to ON position and pull up transistor goes OFF position hence capacitor C_L is discharged through pull down transistor. Like this, due to charging and discharging of load capacitor C_L with pull up and pull down transistors respectively dynamic power occur.

Various techniques are there to reduce static and dynamic powers. They are- Static power can be reduced by run time technique, cache memories and duel threshold techniques. Similarly, dynamic power is reduced by scaling technique, by reduced inter-connections and clock-gating methods.

II. PROPOSED METHOD

A. Clock-Gating:

In a microprocessor for all the peripheral devices like flip-flops, latches and logic gates and address decoders the clock will come from the clock network. At high level the necessary charging and discharging of capacitances when the circuit is idle is avoided by gating the clock to a latch are a logic gate by ANDing the clock with a control signal. Hence the circuit clock power is saved.

Below figure.1 shows the latch element schematic diagram. In this, gate capacitance Cg is the cumulative gate capacitance of a latch. The gate capacitance Cg gets charged or discharged as the clock switches from ON to OFF and OFF to ON, so that the significant amount of power is consumed. Even though the inputs are not changed from present clock position to the next clock position still the power is consumed by the latch.

Figure.2 shows the clock gating, in which the clock is gated by ANDing it with a control signal. In this the clock gate signal is turned off when the latch is not required to switch state and hence the clock does not allow to charge or discharge capacitor, therefore clock power is saved. Using this technique, we can get a net power saving. As the latches of an operand i.e., 32 bit or 64 bit is driven by an AND gate and as we know the capacitance of AND gate itself is soo smaller than the sum of multiple gate capacitance Cg of these latches, net power will be saved.

Figure.3 shows the schematic diagram of dynamic logic gate. The load capacitance CL is connected at the output of circuit. Similarly, at the input Cg capacitance is connected which charges and discharges for any clock cycle and consumes power. Capacitances Cg, CL charged or discharged through PMOS and NMOS transistors. During the pre-charge stage Cg will charge. When it fully charges PMOS goes OFF and NMOS comes to ON, hence load capacitance is charged. During evaluate stage vice-versa, that is Cg is discharged. When it fully discharged PMOS will ON and NMOS goes OFF hence load capacitance is discharged or retains value depending on input to the pull-down network. Capacitance CL consumes power or not depends on the both previous output and current input of the circuit.

Figure 4 shows dynamic logic gate which is being clock gating by clock gate signal. When dynamic logic cell is not used in a cycle, clock gate signal prevents both Cg and CL from switching in the cycle.

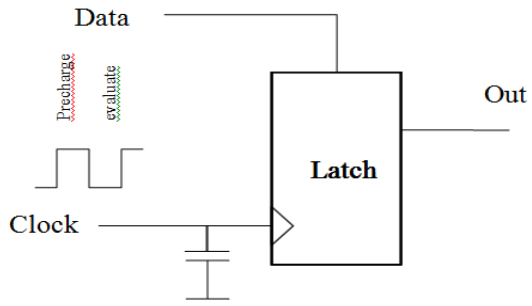

Fig.1 A latch element

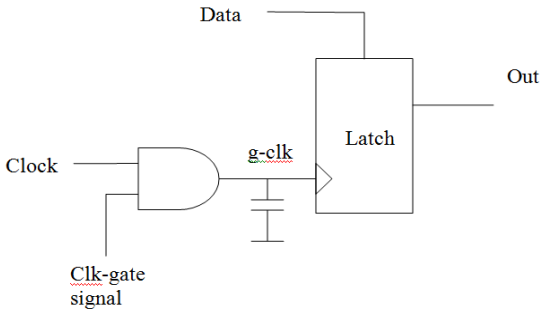

Fig.2 clock gating a latch element

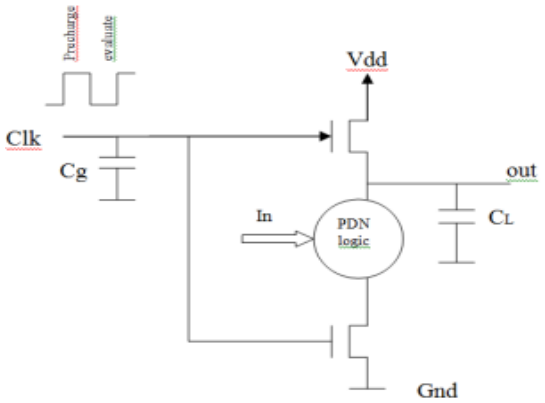

Fig.3 A dynamic logic gate

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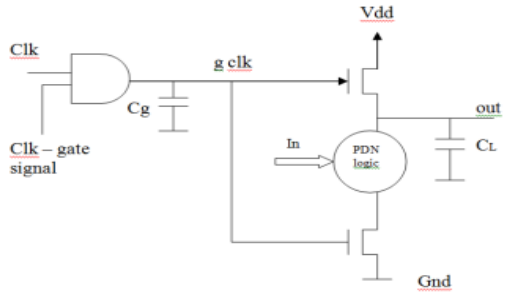

Fig.4 clock gating a dynamic logic gate

This logic reduces unwanted clock power due to Cg and also the dynamic logic power due to C_L.

In this compared with Cg plus C_L, the capacitance due to AND gate is small, hence net power will be saved.

III. DESIGN OF GENERAL PURPOSE PROCESSOR WITH CLOCK-GATING

For every processor while designing its central processing unit we have to design its instruction set first. We have to come to one conclusion with some points like how many instructions we require? what type of instructions they are? and assignment of op-code to each and every instruction is important. After come to conclusion regarding instruction set we have to design data path. Data path will execute various instructions of instruction set. As per processor requirement a tailored cut data path is designed. Hence, while designing data path we have to keep in the mind like number of functions, number of registers, register files and connection for different units etc. After designing above two, at the end we have to design control unit. The control unit passes various control signals to data path. Based on that the logic operations are performed.

The control unit performs operations like fetching, decoding and executing the instructions. The instructions are categorized into different sections i.e., 1.data transfer instructions which are used to move data from accumulator to memory or registers and vice-versa. 2. Arithmetic instructions which perform addition and subtraction operations. 3. Logical instructions which perform basic logic gate operations like NOT, AND, OR, Ex-OR, NAND, NOR etc., 4. Input instructions, these will send data from input devices to CPU. 5. Output instructions, these will collect data from CPU to output devices. 6. Jump instructions, these will change the sequence of operation from one address location to other address location. Unless otherwise memory address as one of its operand, all instructions are encoded by one byte. If memory address is one of its operand then second byte is required for addresses. In the encoding scheme, first four bits are used for opcode. Based on this, opcode has four bits which are identified as two operand instructions, one operand instructions, instructions using of memory address and jump instructions.

A. Data Path:

The data path is designed after completing the instruction set definitions. All instructions in the instruction set are executed by the data path shown in figure 5. The thick lines indicate the width of data path. The width of data path is 8, that is, for data movement 8 bits wide data path is used. As shown in figure 5, thin lines show control lines and all are 1 bit wide except the name is like fddr_$dp_{2,1,0}$ and it indicates many lines.

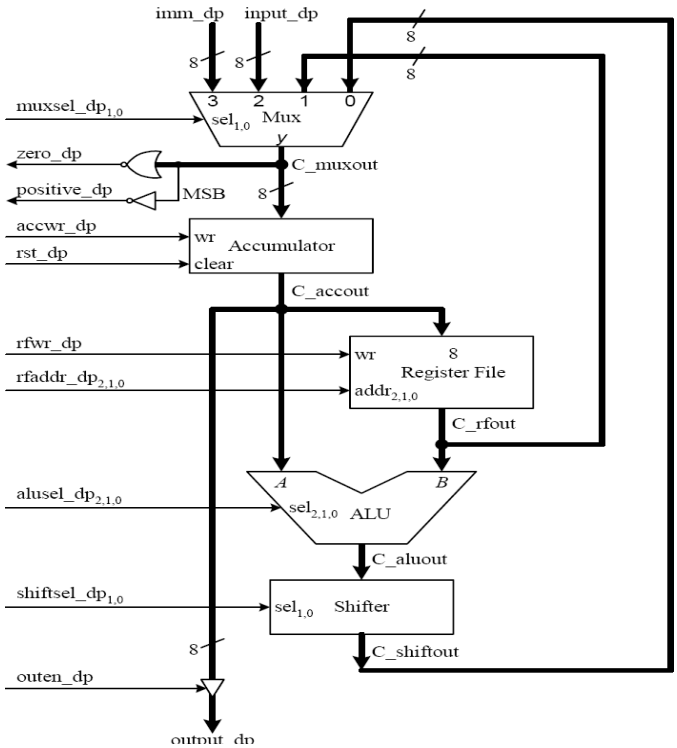

Figure.5 Data path

Flags:

There are two types of conditional flags like zero_dp and position_dp which are being set by two components like NOR gate and NOT gate as shown in figure . For the above two conditions of zero_dp and position_dp, the output of multiplexer will be written into accumulator. To check the zero value 8 input NOR gate is used at the output of multiplexer. To test the number 1, check only MSB of 8 bit values which is by NOT gate.

Accumulator:

The input of accumulator comes from output of multiplexer and it has 8 bit length. Accumulator content will reset by rst_dp and the content of memory or register will write up into accumulator if accur_dp goes high. The output of accumulator goes to output buffer, ALU and register file.

Register file:

Eight locations are there for register file. Each location size is 8 bit length. For reading and writing there are three address lines like rfaddr_dp2, rfaddr_dp1, rfaddr_dp0. Read and write ports are there. Read port is always high which indicates that value from present selected address location. To write selected location rfwr_dp must be used. This is important to note that separate read and write control signals are not needed because we require at a time either read or write.

Arithmetic Logic Unit:

With respect to above data path shown in figure 3, it has 8 operations. The eight operations are selected by 3 select lines as shown like alusel_dp$_{2,1,0}$. i.e., alusel_dp$_{2,}$ alusel_dp$_{1,}$ and alusel_dp$_{0.}$ Depending on instruction the logic will be performed and the output is send to shifter.

Shifter:

The input of shifter is 8 bit length which comes from output of ALU. Based on control lines shown as shift_dp1 and 0, number of positions will be shifted either to left are right depending on operations and then the output will be sent to input of multiplexer.

Output buffer:

Output buffer is a register to which input comes from accumulator. The data will be controlled by outen_dp. The final result of particular operation will be stored in this output buffer. At the end it will be sent to output devices.

Control word:

For the data path shown in figure 5, control word bit length is 14. This control word maps the different data paths come by the control signals.

B. Control Unit:

Below figure.6 shows the control unit of the finite state machine. It consist of various states like reset state, fetch state, decode state and execute state. The operation under particular state is given below-

Reset:

When the reset signal is high, finite state mission starts its execution. On reset signal is high, all its control signals and working variables are initialized. For example, variable are- IR state and program counter etc. Apart from this, the program for execution is also loaded in memory.

Fetch:

When the fetch state is activated, the content of memory location which is being indicated by program counter will be loaded into instructions register. To fetch the next instruction the program counter will be incremented immediately by 1. Sometimes the fetched instruction may be jump instruction, at that time the program counter will change its content accordingly.

Decode:

The content of the instruction register is decoded as per encoding specified by processor. This process will be accomplished in VHDL by the switch condition as opcode. From various cases the state that is exiting respective instruction, is allotted to the next state variable hence the new instructions will be executed starting from the beginning of clock cycle.

Execute:

This state will set up the control word. The control word assigns certain control signals for data path to act accordingly. Every instruction contains its own execution state. Data path will not take it's action for all jump instructions.

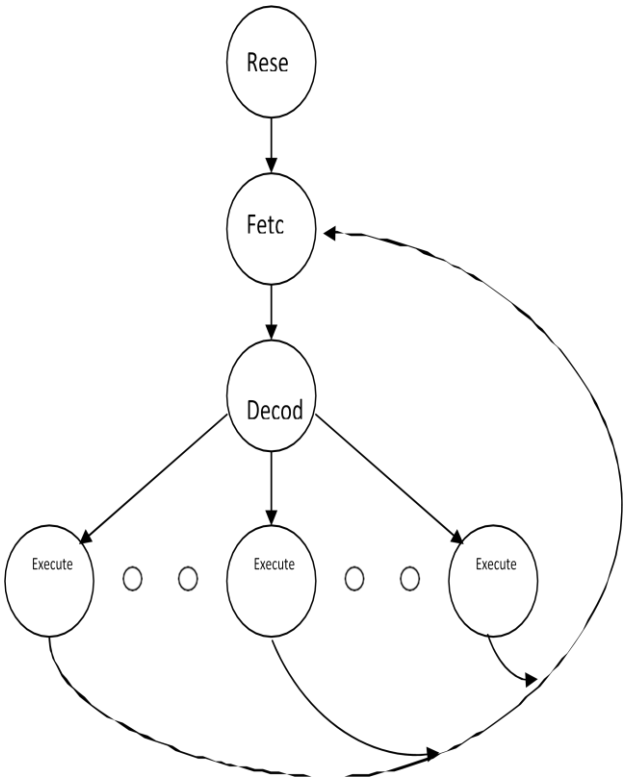

Figure.6 State diagram for the control unit.

C. Complete Processor:

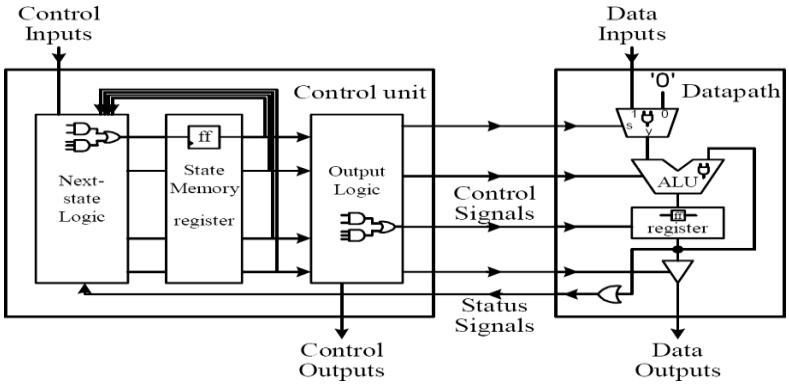

Figure.7 Complete general purpose processor

Figure.7 shows the architecture of complete general purpose processor. It consists of control unit and data path blocks as the main units. Control unit block consists of next state logic, storage memory register and output logic. Present state of the logic circuit will be stored by state memory resistor based on the present state logic, output logic will be framed and then control signals will be passed to the data path black. While sending the present state logic to output logic the same is fed back to the next state logic. Depending on the control signal which have come from control unit, the data will be manipulated by multiplexer, ALU, register and buffer the final data output is available at the output of buffer. In order to generate the next state, logic state signals will come to next state logic black from the data path block.

IV. SIMULATION RESULTS

Below figure.8 to 13 show simulation results of general purpose processor when with and without clock gate is used. Simulation has been done by Xilinx 13.5 software tool and synthesis by XST with SPARTAN FPGA board.

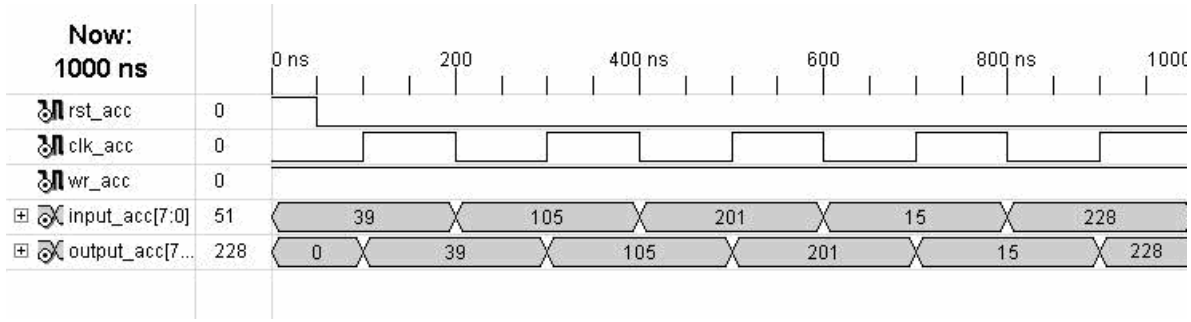

Figure.8. Accumulator output when without clock gate

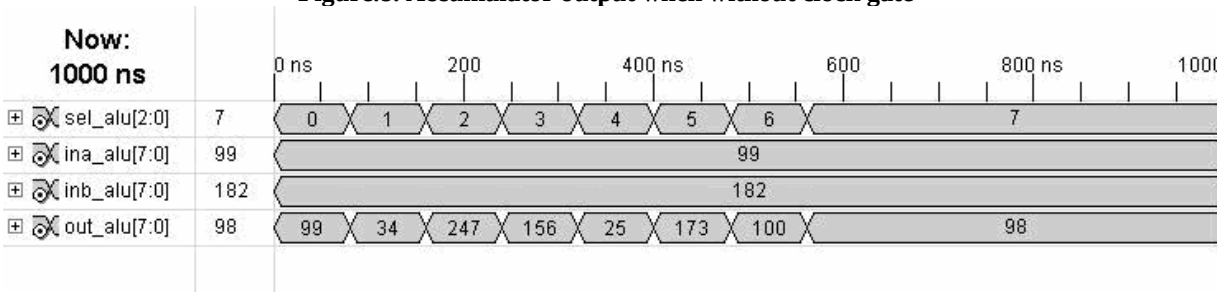

Figure.9. ALU output for without clock gate when the inputs are A = "01100011" and B = "10110110".

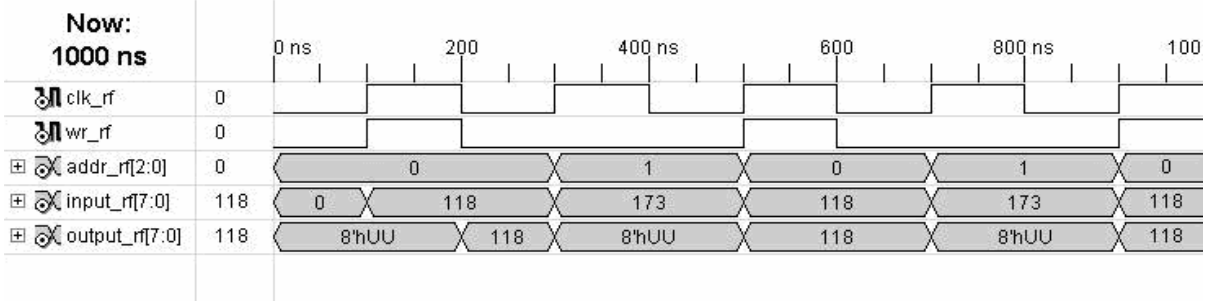

Figure.10. Multiplexer output when without clock gate.

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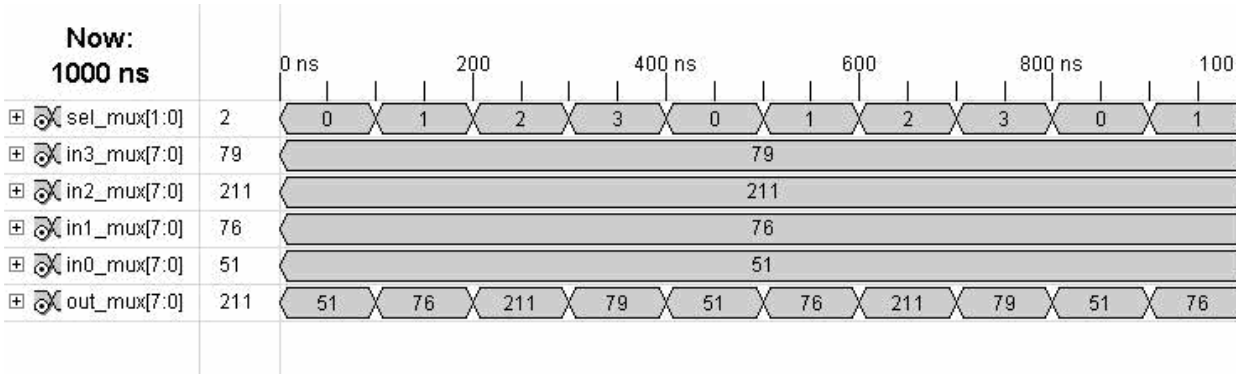

Figure.11. Register file output when with clock gate

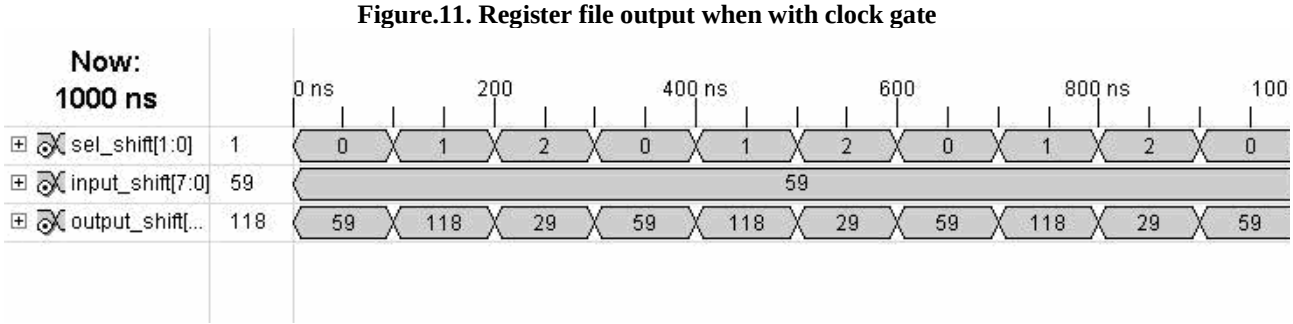

Figure.12. Shifter output for with clock gate when the input is "00111011".

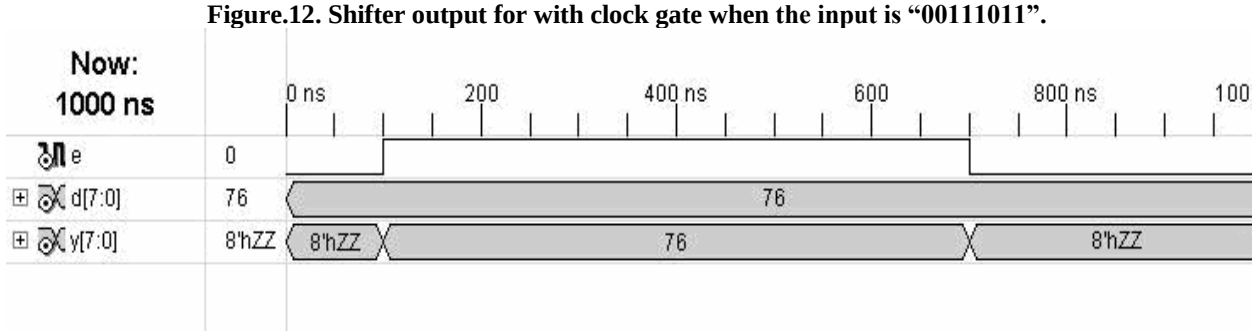

Figure.13. Tri-state buffer output when with clock gate

POWER CALCULATIONS (WITH CLOCK GATE & WITHOUT CLOCK GATE):

	ALU		ACC		MUX		SHIFTER		BUFFER	
	With Out C.G	With C.G	With out C.G	With C.G	With out C.G	With C.G	With out C.G	With C.G	With out C.G	With C.G
No.of slices	26	18	14	9	12	8	10	8	3	1
No. of 4 i/p LUT's	32	25	14	9	20	16	11	9	3	1
No. of IO's	35	27	24	19	56	42	24	18	22	17
No. of IO Buffers	35	27	24	19	56	42	24	18	22	17

Table.1 Cell Usage for the General Purpose Processor

V. CONCLUSION

Even though portable batteries like Lithium, Cadmium can give the more durability, design engineers had found the various techniques like parallel processing, pipe lining, scaling etc., to consume the less power by the VLSI circuits so that power sensitive packs could work for more and more run time. All those techniques have its own limitations. To avoid those limitations and to give more durability to power packing devices, similarly to consume less power by the general purpose processors clock-gating technique which is a novel technique applied and proven that power consumption is less with clock gating compared to without clock gating.

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Dr. R. Prakash Rao, received Ph.D from JNTUH, Hyderabad; M.Tech from College of Engineering Andhra University, Vizag and B.Tech from Nagarjuna University, Guntur, India. He has 17 years of teaching experience. He worked as Professor & HOD in the department of ECE, St.Peter‟s Engineering College, Hyderabad for 8 years. Presently he is working as Professor & BOS Chair in the department of ECE, PACE ITS, Ongole. He published 19 papers in various National and International reputed Journals and Conferences. He got best faculty award for the A.Y 2017-2018 by the Rotaract club, Secundrabad. He has guided 14 M.Tech projects and about 32 B.Tech projects in various fields. His research interest includes VLSI, VLSI with signal processing, Microwave Engineering and Embedded Systems.

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