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Run-Time Re-configuration using FPGA for Bio-Medical Application

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ABSTRACT

Now-a-days, FPGAs are even used as prototyping devices. With the ongoing technologies to build these devices, FPGAs are becoming larger, faster and more accurate. With the proper development environments, FPGAs can also be used in end products to provide specialized features that are not always possible with ASIC chips such as in-field updates of hardware. Partial Re-configuration can be used to maximize the resource utilization in FPGAs. The partial re-configuration with FPGA can be used in Bio-Medical application at run-time. This application can be considered to monitor and measure various health parameters viz., Body-Temperature, Heart Rate, ECG, Oxygen Saturation and Blood-Pressure etc. In this research article, the runtime partial reconfiguration using VHDL coding in Xilinx tool has been performed.

Keywords: *Partial Reconfiguration, FPGA, Dynamic partial reconfiguration, Static partial reconfiguration, Application Specific Integrated Circuit (ASIC)*

I. INTRODUCTION:

The important feature of the FPGA is partial reconfiguration (PR), it is further sub divided into two types: Dynamic partial reconfiguration (DPR) and Static Partial Reconfiguration. When the device is in passive state the reconfiguration takes area in the static partial reconfiguration. In DPR, the device is partially reconfigured while the rest of FPGA is yet running. Partial reconfiguration is a step where some section of FPGA gets reconfigured after its initial configuration.

The partial re-configuration using FPGA can be used in Bio-Medical application at run-time. This application is used to monitor and measure various health parameters viz., Body-Temperature, Heart Rate, ECG, Oxygen Saturation and Blood-Pressure etc. The Xilinx tool is used to reconfigure FPGA at runtime using various biomedical sensors for different health parameters.

FPGA's allows the thinking of gate-arrays the place the developer can operate flip flops, logic gats and built in storage. Runtime partial reconfiguration is also significant for Bio-medical application. Major reasons to shift to FPGA include the following aspects: improve execution time, increase in privacy, elimination of positive embedded constraints – restrained power consumed, and precise event disturbance protection [7]. Along with these there is increase in control performance; execution time is decreased dynamically reconfiguring it.

II. PREVIOUS WORK:

In wireless body sensor networks (WBSNs), sensors continuously monitor human physiological activities using medical sensors, for example; blood pressure, body temperature and electrocardiography (ECG). A WBSN can be used to develop a patient monitoring system. The traditional body sensor networks (BSNs) have limited hardware resources in terms of computational capabilities, data processing speed, and memory and battery life. Also these BSNs are generally not suitable for the implementation of security mechanisms, reason is that, implementation of security mechanisms require relatively more hardware resources because of the complexity of their algorithms. To get rid of these limitations a Field Programmable Gate Array (FPGA) device is suitable

because of its flexible architecture and high performance features. In this paper an FPGA based experimental framework is investigated to implement real time body temperature monitoring with reliable data transmission, using data integrity verification. The data integrity verification is achieved using newly selected cryptographic hash function called, SHA-3 (Secure Hash Algorithm-3).by Rao M [2] et al.

To extract the Fetal Electrocardiogram (FECG) signal from the mother's abdomen signal which is an important signal to analyse the abnormalities of the fetal heart by a physician. Fetal ECG is extracted from the mother's domen by using least-mean-square (LMS) adaptive filter based on the FIR filter coefficients. This FECG is used to calculate the fetal heart beat and the period of the signal based on our estimation. To take FECG in real time, maternal woman should wear a wide belt around her abdomen which is fitted with several ECG electrodes. The data collected from the electrodes are sent to a system and then analysed with the help of adaptive noise canceller algorithm, which is used to separate the signals. by Rasu R [1] et al.

Dynamic partial reconfiguration (DPR) is a technique that optimizes resource utilization of SRAM-based FPGAs, since it allows changing, on the fly, the functionality of a portion of its logic. A common DPR development flow requires the use of, at least, a microprocessor and several development tools (EDK, XSDK, Plan Ahead); moreover, proposals are mainly based on Micro Blaze, ARM or PowerPC embedded processors, which also require extra memory control blocks. This article presents a generic DPR manager IP core (Intellectual Property), whose versatility allows the use of either any embedded processor or simple control logic. Results in terms of reconfiguration time and resources for Virtex 5 and Virtex 6 SRAM-FPGAs show its advantages and interest over traditional solutions. by Souvik Das [3] et al.

This paper based on Real Time Health Monitoring System using Arduino. In this paper, researcher implemented a prototype model for the real time patient monitoring system. This method is used to measure the physical parameters like body temperature, heart beat rate, and oxygen level monitoring with the help of different biosensors. In this novel system the patient health is continuously monitored and the acquired data is transmitted to a using Wi-Fi wireless sensor networks. Transmission and reception of the signal is done by using HT12D & HT12E is a 212 series decoder IC (Integrated Circuit) for remote control applications manufactured by Holtek. It is commonly used for radio frequency (RF) wireless applications. By using the paired HT12E encoder and HT12D decoder one can transmit 12 bits of parallel data serially Rajalakhshmi.S [4] et al.

Since the implementation of partial reconfiguration at FPGAs has been taken place, more opportunities appeared to take the advantages of dynamic reconfiguration especially in SDR implementation. McDonlad [5] provides an overview of reprogrammable Forward Error Correction (FEC) for partial reconfiguration design on Virtex-4 and comments on the additional overhead necessary for creating such a design. Also in [6], Delahaye and Palicot are focusing on implementation of Convolutional Coder, a constellation mapper, and FIR filter. They implement management architecture based on MicroBlaze interconnected with a NoC which is extended from a 3G wireless communications system.

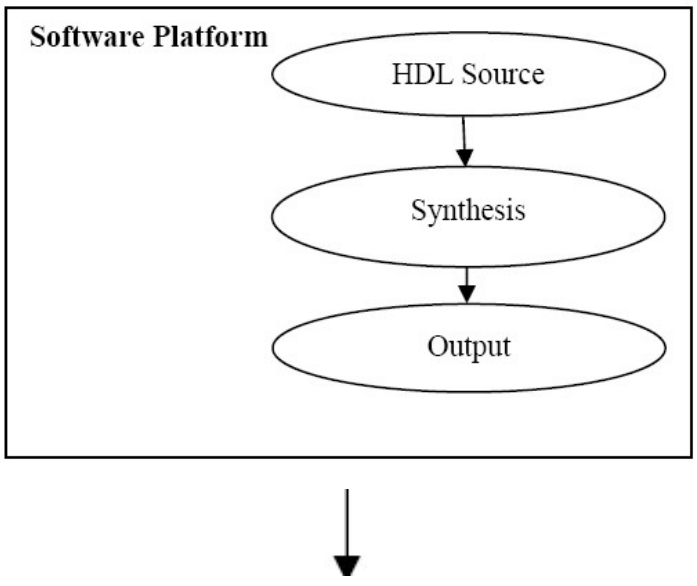
III. PROPOSED WORK:

The proposed work flow shall be carried out as following manner.

1) **Software platform:** It consists of

- HDL Source and Synthesis
- Output waveform

2) Hardware Platform



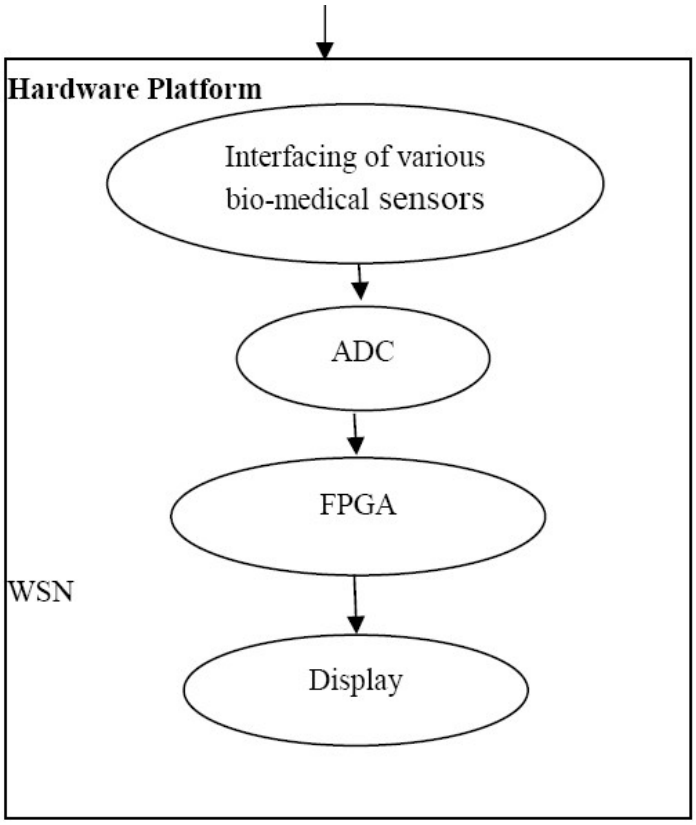


Fig. No. 3.1 Work flow

In this paper, a software implementation part is discussed, using Xilinx platform. In this section, the HDL source has been successfully compiled and run at runtime for Partial Reconfiguration using FPGA for our Bio-medical application. In second part the hardware platform gets implemented using FPGA 7 series board and various biomedical sensors; and the output will be displayed using WSN or IoT.

3.1 DYNAMIC PART:

In the entire lifespan of utility dynamic components are not required to be lively as a result stated unbiased components of input design. Into the internal part of target machine modules share common areas; as it is assumed that the modules do no longer require walking parallel with different modules in the application at run-time. Changes might also exist that the modules are saved internal the reminiscence avail in the FPGA.

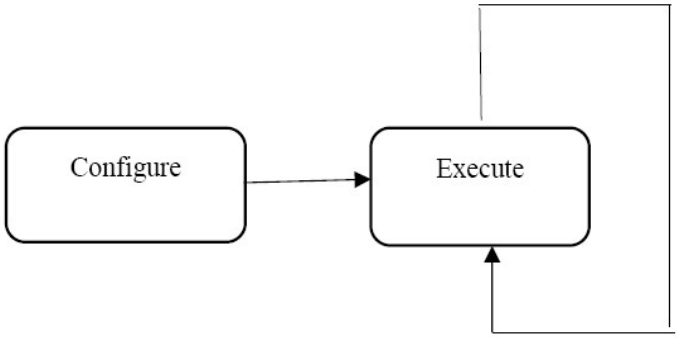


Fig. No. 3.2 Dynamic Part

3.2 STATIC PART:

Parts that stay lively throughout the run-time of the application are generally the static section for an input design. Always kept interior the static vicinity of target and running all the time entire trendy inputs and outputs of the system are achieved be the static modules speaking to the dynamic modules through fixed interfacing. The structure of system is modified using partial bit stream while the final of the program continues the run the similar way as earlier than programmed.

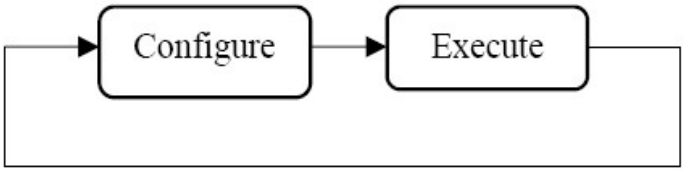


Fig. No. 3.3 Static Part

3.3 ABILITY TO CHANGE HARDWARE:

Fractional reconfiguration makes the client convenient to help without trouble and enhance equipment in the subject area. FPGAs are advantageous to change whenever, locally or remotely.

The snap-shot below shows the Xilinx simulation process, in this process the Top-level module and RTL schematic displayed after the implementation task.

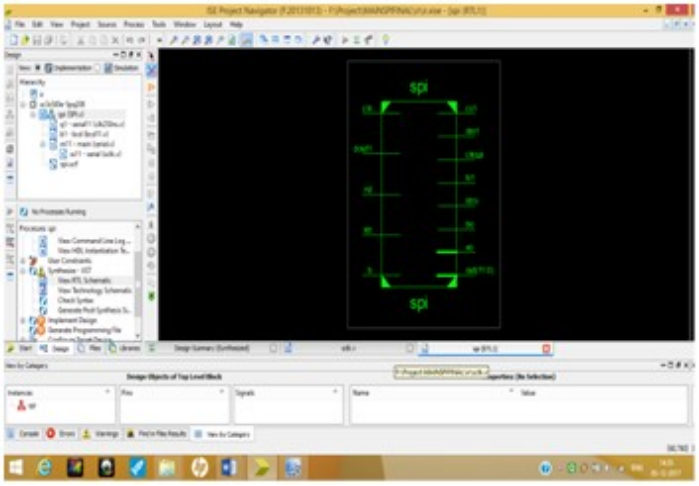


Fig No. 3.4 Top-Level module

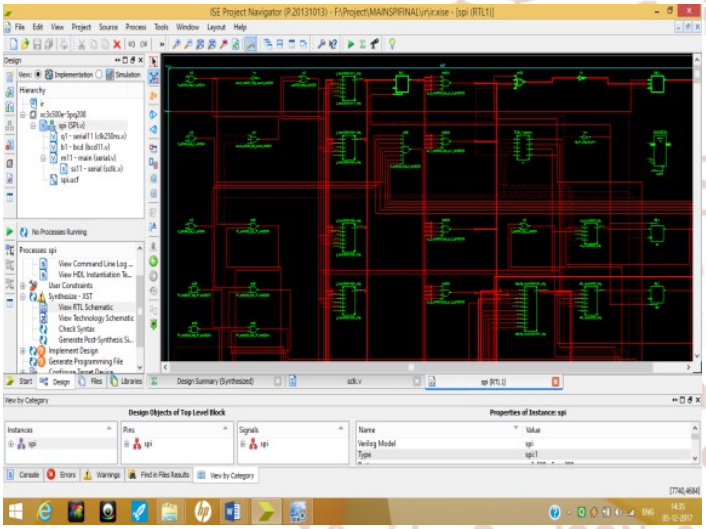


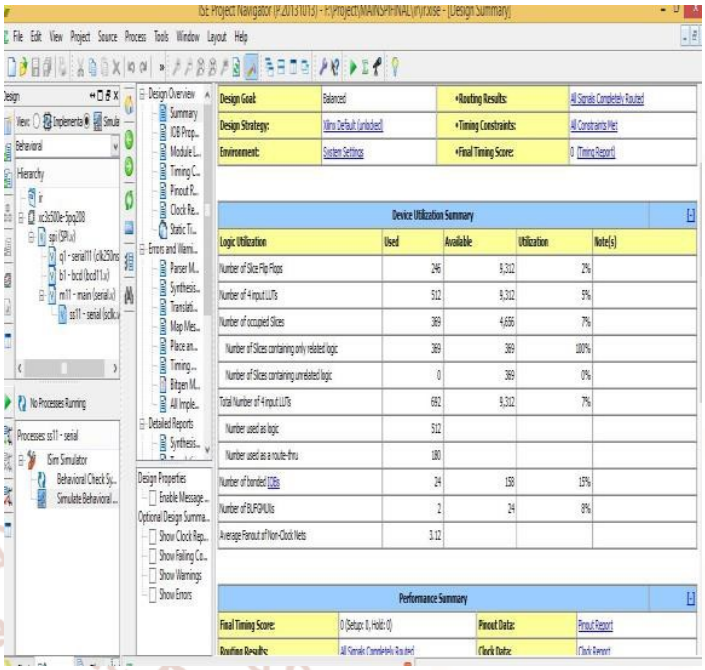
Fig No. 3.5 RTL schematic

IV. RESULT:

After synthesis and simulation we are able to see

1. Output waveform: The output waveform shows the timing diagram of reconfiguration process in to the Xilinx tool. In this process in future when the sensors are connected to FPGA platform the complete reconfiguration output can be seen.

2. Device Utilization: It shows how many resource gets used for this particular program i.e. Number of flip-flops used, number of slices used and so on. As compared to previous method while using PR the required device utilization is less; so it saves execution time as well as resources.



Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	All Constraints Met
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	246	9,312	2%	
Number of 4 input LUTs	512	9,312	5%	
Number of occupied Slices	369	4,656	7%	
Number of Slices containing only related logic	369	369	100%	
Number of Slices containing unrelated logic	0	369	0%	
Total Number of 4 input LUTs	692	9,312	7%	
Number used as logic	512			
Number used as a route-thru	180			
Number of bonded IOBs	24	158	15%	
Number of BUFG/BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.12			

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report

Fig. No. 4.1 Device Utilization Summary

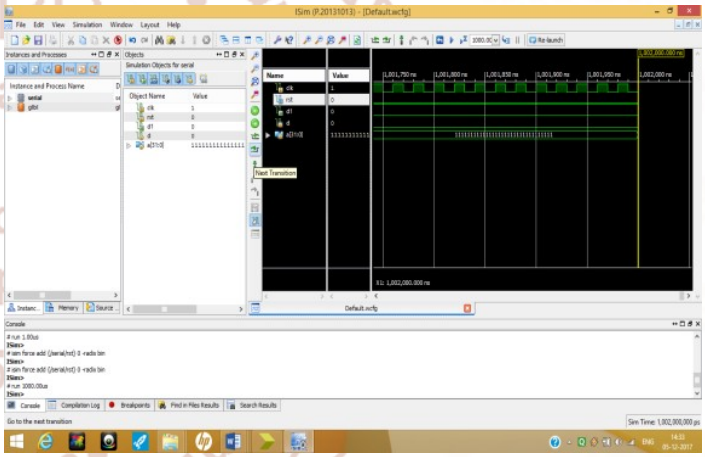


Fig No. 4.2 Output waveform

V. CONCLUSION:

In this research article, the Run-time partial reconfiguration using FPGA has implemented for Bio-Medical application. It shows how much resource is utilized for this operation. The resource utilization is verified with reference paper [8] the number of slices used is 1056 and frequency required is 158.90 MHz, here in this paper number of slices used for this operation is 246 and the total number of 4 unit LUTs are used is 692, indirectly it will improve security, accuracy, compatibility and the actual area (slots) of the device used. The output waveform shows the timing diagram of reconfiguration done for application. As a part of this system, for run-time reconfigurable platform Verilog hat code for further

work i.e. to reconfigure FPGA and our proposed system.

VI. FUTURE DISCUSSION:

In future, various Bio-medical sensors are get connect to patient's body and the Partial Reconfigure of FPGA can be performed as per requirement. The output data will be collected and send through WSN at remote location. Here in this, for future scope we may use the IoT based system for sending and receiving data.

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