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Study on Modulation Strategy of Electronic Converters Based on Improved D-NPC Topology for Full Electric Vehicle

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Abstract: The battery is the only power source of full electric vehicles, and the converter plays a key role in power and signal conversion; therefore, the stability and reliability of the converter determine the performance of the whole vehicle system. In order to improve the overall performance of the converter and optimize the function of the ID-NPC (improved diode neutral-point-clamped) topology with power allocation, the two-level topology is improved, and it is also a part of the ID-NPC topology. Based on the ID-NPC topology, the converter level can switch according to the proposed three-level and two-level modulation conversion strategies, which extends the fault-tolerant function of the converter. Finally, a simulation and experimental platform is built to verify the function of the improved topology and the feasibility of the proposed modulation strategy.

Keywords: electronic converter; improved two-level; ID-NPC; modulation strategy

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1. Introduction

Environmental and resource problems are two prominent contradictions that perplex the development of the automobile industry. The emergence of electric vehicles indicates the direction to solve these two problems [1]. The battery, converter, and driving motor are three important parts of an electric vehicle. Many scholars have conducted research on batteries, especially in the charge and discharge states [2,3]. Now, most drive motors use a permanent magnet synchronous motor. The power electronic converter is a more important component, and the topology has developed from two-level to multilevel.

The waveform quality of the output voltage is greatly improved by using a multilevel topology converter [4]. At present, the main structures of the multilevel converter are of the cascade type and NPC (neutral-point-clamped) type. The earliest NPC form of an element is the FC-NPC (flying-capacitor neutral-point-clamped) topology [5]. According to the structural characteristics of FC-NPC, a bidirectional switching power device is used to replace the capacitive devices as a neutral-point-clamped element, similar to the "T" shape, which is called the T topology [6]. The D-NPC (diode neutral-point-clamped) topology was proposed based on the T-NPC and FC-NPC topologies [7]. The D-NPC converter is featured by a simple main circuit, a flexible control mode, and easy control of the direction of the energy flow and power factor [8]. However, the inherent control and driving method of D-NPC are attributed to its uneven heat loss, increasing the design difficulty of a radiator, and limiting the power level, output current, and switching frequency. In order to improve the loss distribution, the A-NPC (active neutral-point-clamped) topology was proposed subsequently, but the added number of switching elements also brings about increased conduction loss and switching loss [9]. The comparison of four traditional topologies is shown in Table 1 [10]. As it can be seen from the table below, the switching loss of the two-level topology is large, but the heat distribution is balanced and different than that of the D-NPC topology.

Table 1. The comparison of four traditional topologies.

Topological Structure	Two-Level	D-NPC	A-NPC	T-NPC
Number of IGBT	2	4	6	4
Number of driving paths	2	4	6	4
Number of diodes	2	6	6	4
Device withstand voltage	V_{dc}	$V_{dc/2}$	$V_{dc/2}$	Horizontal switch: $V_{dc/2}$ Vertical switch: V_{dc}
Control difficulty	Easy	More difficult	Most difficult	More difficult
Withstand voltage	No	Capacitance	Capacitance	Capacitance
Output level	2	3	3	3
Conduction loss	Minimum	Large	Large	Maximum
Switching loss	Large	Low	Low	Maximum
Heat distribution	Balance	Imbalance	Algorithmic balance	Balance

2. D-NPC and ID-NPC Topology Converter and Loss Allocation Analysis

2.1. Traditional D-NPC (Diode Neutral-Point-Clamped) Topology

The D-NPC topology was proposed in 1980, which is more suitable for medium-voltage applications. The topological structure is shown in Figure 1 [11,12]. Each main bridge arm consists of four controllable switching elements and two clamped elements. The power supply is composed of two groups of DC sources with a single voltage of $V_{dc/2}$ in series, and the neutral point of the DC source is connected with the neutral point of the series diode. Taking the first group of main bridge arms as an example, when the first element T_{11} and the second element T_{12} of the four elements of main bridge arms are connected, the output voltage is $V_{dc/2}$ (called the positive-level state); when the second element T_{12} is connected with the third element T_{13}, the output voltage is 0 (called the zero-level state); when the third element T_{13} is connected with the fourth element T_{14}, the output voltage is $-V_{dc/2}$ (called the negative-level state). Four controllable switching elements turn on in turn to make the output present the three-level state. In the process of switching from the positive-level state to the zero-level state and from the zero-level state to the negative-level state, the second and third elements are in a repeated conduction state, that is, a continuous state, and the heat distribution on the single device is uneven [13,14]. Since each bridge arm has four elements, each element needs one driving circuit, and a set of converters needs 12 driving circuits [15,16].

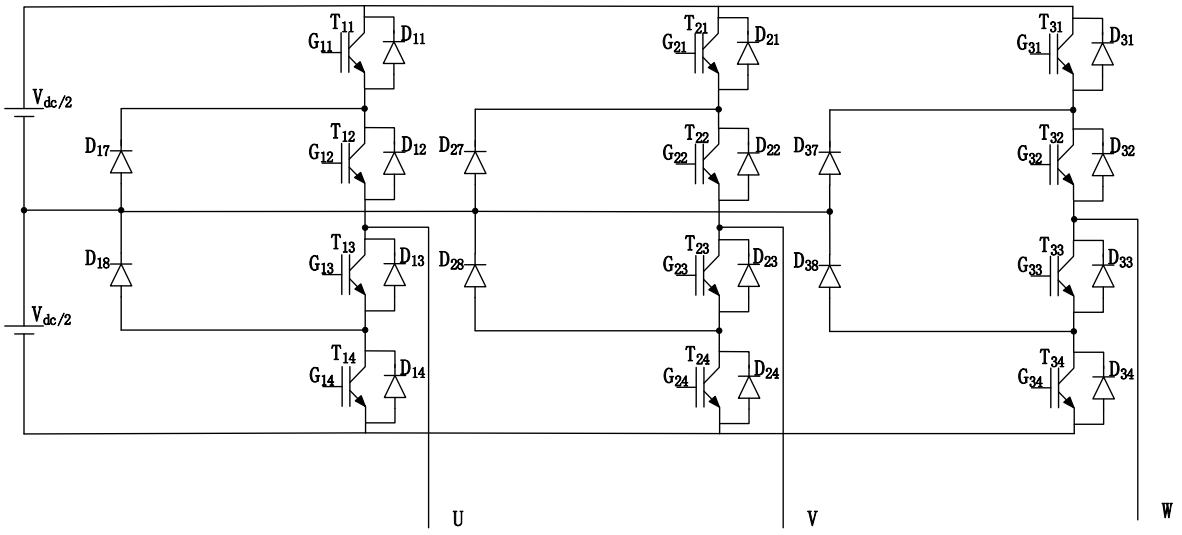

Figure 1. Traditional D-NPC (diode neutral-point-clamped) topology.

2.2. D-NPC (Diode Neutral-Point-Clamped) Switching States

The switching states of the D-NPC topology are shown in Table 2. The switching table

is explained by the U-phase.

Table 2. D-NPC (diode neutral-point-clamped) switching table.

Switching	G_{11}	G_{12}	G_{13}	G_{14}
"+"	1	1	0	0
"0"	0	1	1	0
"−"	0	0	1	1

2.3. ID-NPC (Improved Diode Neutral-Point-Clamped) Topology

ID-NPC (improved diode neutral-point-clamped) is shown in Figure 2. Each bridge arm consists of six controllable switching elements and two clamped elements. The connection mode of the DC power supply and converter is the same as that of D-NPC. Taking the U-phase as an example, the six switching elements of the bridge arm are divided into three groups: T_{11} and T_{12}, T_{13} and T_{14}, and T_{15} and T_{16}, and the driving ports are G_{11}, G_{13}, and G_{15}, respectively. When the driving port G_{11} is connected, the output voltage is $V_{dc/2}$ (positive state); when the driving port G_{15} is connected, the output voltage is 0 (zero state); when the driving port G_{13} is connected, the output voltage is $-V_{dc/2}$ (negative state). Three groups of switching elements turn on to make the output voltage present the three-level state. During switching states, the positive state, zero state, and negative state are completed by independent components, with no overlapping, meaning the heat distribution is uniform. The three groups of elements need three driving circuits, and the converter needs nine driving circuits.

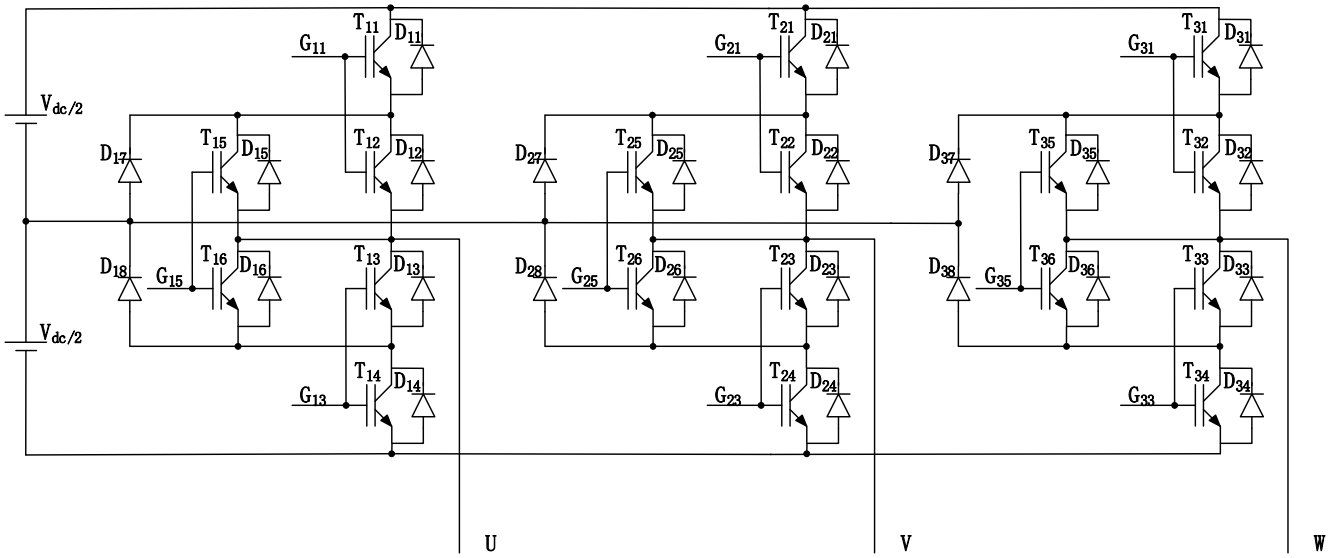

Figure 2. The ID-NPC (improved diode neutral-point-clamped) topology.

2.4. ID-NPC (Improved Diode Neutral-Point-Clamped) Switching States

Corresponding to the ID-NPC topology, the switching states table is shown in Table 3. The switching states are simplified and more intuitive. The switching table is explained by the U-phase.

2.5. Analysis of D-NPC (Diode Neutral-Point-Clamped) Switching Loss

It is also different that the different operating points and different modulation application schemes determine the loss and temperature distribution of each device. The following analysis takes the U-phase in three phases as an example [17].

Table 3. ID-NPC switching table.

Switching	G_{11}	G_{15}	G_{13}
"+"	1	0	0
"0"	0	1	0
"−"	0	0	1

The boundary of the D-NPC converter's working area is the most critical working point. According to whether the reference direction of the current and the voltage is the same or not, the factor α is +1 or −1. The maximum modulation depth is M = 1.15, and the minimum is M ≈ 0. Based on these conditions, the switching process can be divided into four types: D1 (α =+1, M = 1.15), D2 (α = −1, M = 1.15), D3 (α = +1, M ≈ 0), and D4 (α = −1, M ≈ 0) [18].

For the D1 type (α = +1, M ≈ 0), α = +1, the voltage and current directions are the same, M = 1.15, and the converter state switches between "+" and "0", as shown in Figure 3. T_{11} turns off and D_{17} turns on, and T_{12} bears the half-wave phase current in the whole switching process. In the case of maximum modulation M, T_{11} has on-loss at the beginning of switching and current loss at the end of switching. D_{17} has smaller conduction loss and self-loss after conduction. The solid line represents the current path direction in the "+" state, the dotted line represents the current path direction in the "0" state, and the thickness of the solid line and the dotted line represents the duty cycle.

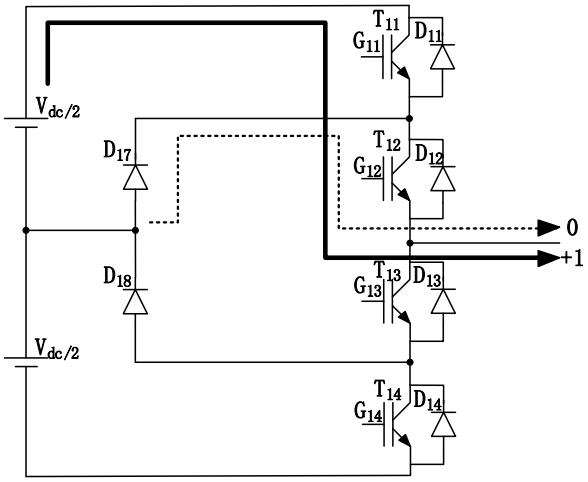

Figure 3. D1 type (α = +1, M ≈ 0).

For D2(α = −1, M = 1.15), as shown in Figure 4, the actual current shifts 180 degrees from the direction shown in the figure, the converter switches between "0" and "−" states, and T_{12} and T_{13} have switching losses. After switching to the "−" state, the reverse diodes D_{13} and D_{14} are connected in series, and the two are on after switching, with negligible switching loss. When the state switches from "−" to "0" states, D_{14} or D_{13} has reverse recovery loss. T_{12} needs to turn the current on and off in the "0" to "−" states and bears a large on and off loss. When the reverse recovery loss occurs in D_{14}, the loss scale for D_{14} and T_{12} also depends on the duty cycle of both. When the lower current is reversed, for T_{14}, the internal switch and diode have loss, and the two also have an obvious junction temperature in the same housing.

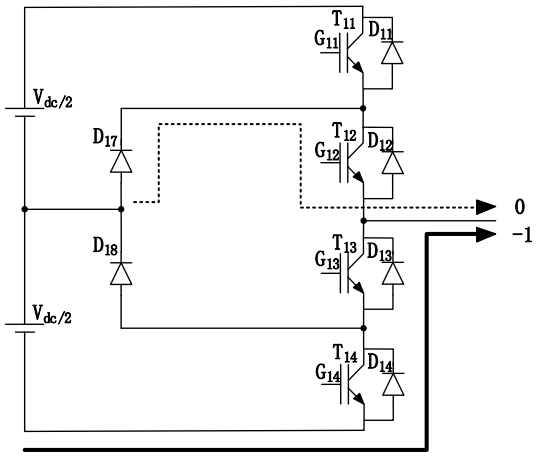

Figure 4. D2 type ($\alpha = -1$, M = 1.15).

For the case of the D3 type ($\alpha = +1$, M $\approx$ 0), as shown in Figure 5, different from the D1 type, the conduction loss is different due to the change in the duty cycle. D_{17} has a negligible turn-on loss, directional recovery loss, and large duty cycle turn-on loss.

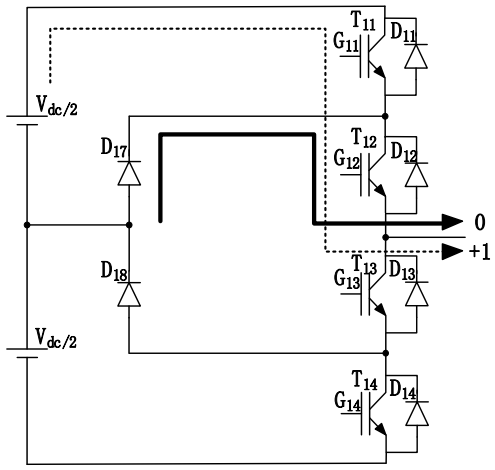

Figure 5. D3 type ($\alpha = +1$, M $\approx$ 0).

For the D4 type ($\alpha = -1$, M $\approx$ 0), as shown in Figure 6, D_{17} and T_{12} have a current most of the time. T_{12} has conduction and turn-off loss. Due to the large duty cycle, the conduction loss is also large. D_{13} and D_{14} also bear reverse recovery losses when off.

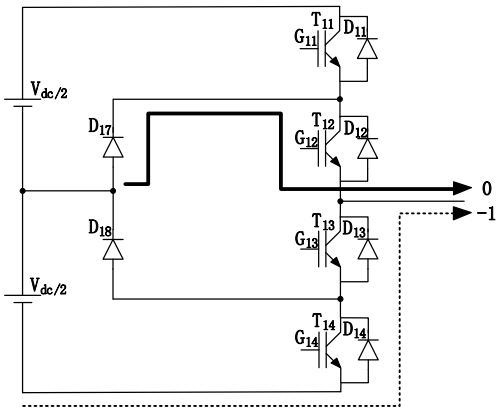

Figure 6. D4 type ($\alpha = -1$, M $\approx$ 0).

2.6. Analysis of ID-NPC (Improved Diode Neutral-Point-Clamped) Switching Loss

In order to facilitate the comparison with D-NPC switching loss, the working point setting of the ID-NPC converter is the same as that of D-NPC, and the analysis method is the same as above. The four types are marked as the ID1 type ($\alpha = +1$, M = 1.15), ID2 type ($\alpha = -1$, M = 1.15), ID3 type ($\alpha = +1$, M $\approx$ 0), and ID4 type ($\alpha = -1$, M $\approx$ 0) [19].

For the ID1 type ($\alpha = +1$, M = 1.15), the state switches between "+" and "0", as shown in Figure 7. T_{11} and T_{12} switch with D_{17} and T_{15}. T_{11} and T_{12} are off and bear the turn-off loss. The mechanism is the same when opening, and the two pipes bear the turn-on loss. T_{15} bears the conduction loss. After conduction, T_{15} bears the half-wave phase current. The solid line represents the current path in the "+" state, the dotted line represents the current path in the "0" state, the thickness of the solid line and the dotted line indicates the duty cycle, and the arrow direction is the current direction. Compared with the type D1 switching loss in Figure 3, the circuit switching has one more on–off loss.

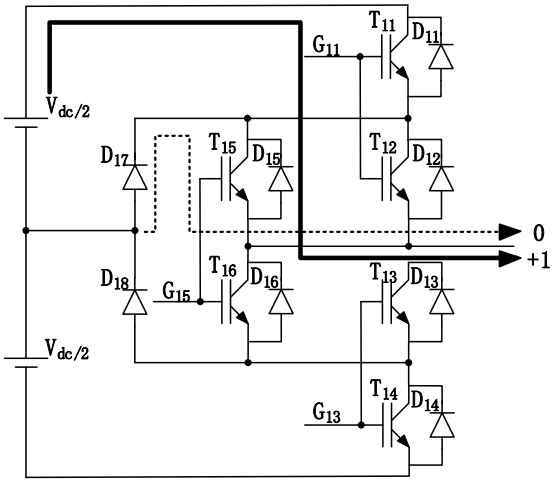

Figure 7. ID1 type ($\alpha = +1$, M = 1.15).

For the ID2 type ($\alpha = -1$, M = 1.15), as shown in Figure 8, the actual current is also 180 degrees phase shifted with the direction shown in the figure, and the converter switches from "0" to "−" states. T_{15} is off, then D_{17} is off, and after the dead time, T_{13} and T_{14} are on. On the contrary, D_{13} and D_{16} or D_{14} bear large reverse recovery loss. T_{15} needs to turn the conduction current on and off when switching and bears the on–off loss. Due to the different duty cycles, for D_{13} and D_{16}, D_{14} and T_{15}, and D_{17}, the loss is different.

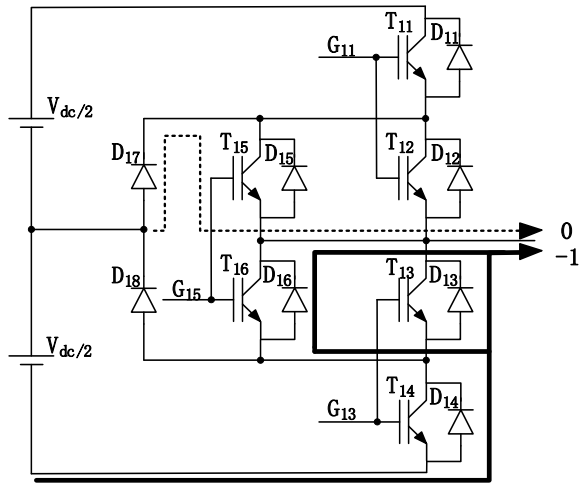

Figure 8. ID2 type ($\alpha = -1$, M = 1.15).

In the case of the ID3 type ($\alpha = +1$, $M \approx 0$), as shown in Figure 9, it switches from "+" to "0", T_{11} and T_{12} turn off, and T_{15} turns on. In the switching process, T_{11} and T_{12} have on and off losses. Different from D3, T_{15} has on and off losses. Due to the different duty cycles, the conduction loss is also different.

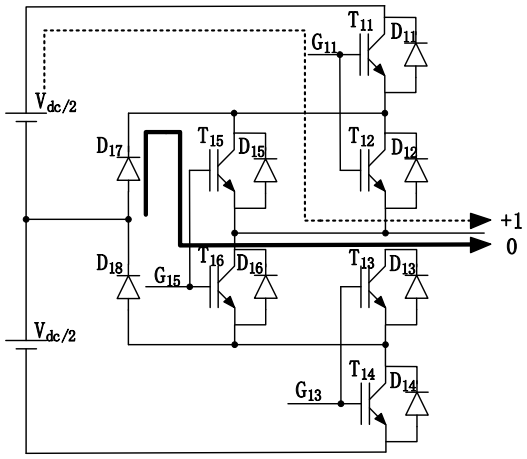

Figure 9. ID3 type ($\alpha = +1$, $M \approx 0$).

For the ID4 type ($\alpha = -1$, $M \approx 0$), as shown in Figure 10, the difference compared with ID2 is that duty cycles lead to different conduction losses. In the "−1" state, because D_{14} is connected in series with D_{13} and D_{16}, the three diodes conduct at the same time when they are on, and there are reverse recovery losses when they are off.

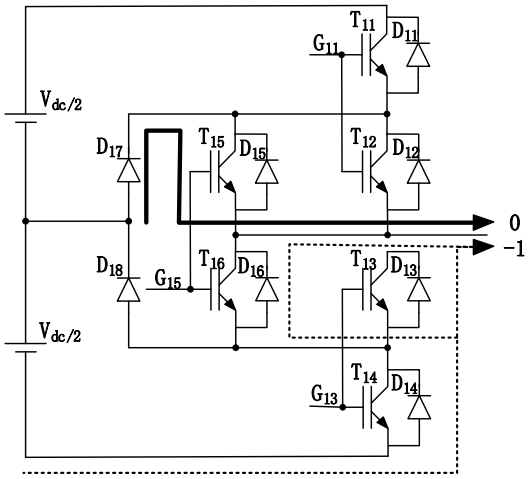

Figure 10. ID4 type ($\alpha = -1$, $M \approx 0$).

2.7. Comparison and Analysis

The above analysis is summarized in Tables 4 and 5.

Table 4. D-NPC switching loss table.

α	M	T	State	T_{11}	D_{11}	T_{12}	D_{12}	T_{13}	D_{13}	T_{14}	D_{14}	T_{15}	D_{15}	T_{16}	D_{16}	D_{17}	D_{18}
+1	1.15	D1	"+"⟷"0"	√				○								○	
−1	0	D2	"0"⟷"−"			√		○	○	○	○					√	
+1	1.15	D3	"+"⟷"0"	√				○								○	
−1	0	D4	"0"⟷"−"			√		○	○	○	○					√	

"√" represents off–on loss and "○" represents on–off loss.

Table 5. ID-NPC switching loss table.

α	M	T	State	T_{11}	D_{11}	T_{12}	D_{12}	T_{13}	D_{13}	T_{14}	D_{14}	T_{15}	D_{15}	T_{16}	D_{16}	D_{17}	D_{18}
+1	1.15	D1	"+"⟷"0"	√		√						○		○		○	
−1	0	D2	"0"⟷"−"					○	○	○	○	√		√	○	√	
+1	1.15	D3	"+"⟷"0"	√		√						○		○		○	
−1	0	D4	"0"⟷"−"					○	○	○	○	√		√	○	√	

"√" represents off–on loss and "○" represents on–off loss.

Comparing the switch loss tables, the conclusions are as follows:

1. The ID-NPC topology only needs nine driving circuits.
2. ID-NPC has two more elements per phase, and six more elements in three phases.
3. The ID-NPC topology has more switching loss in no-load switching.
4. The additional switching elements of ID-NPC can evenly distribute the heat generated by switching loss, and the heat distribution is relatively more uniform.
5. ID-NPC can run in the two-level state, when G_{12} is zero (take the U-phase as an example). This is very suitable for the field of zero speed in the power drive system, and the characteristic is that the regulation system is low, and the frequency output is zero or near zero.
6. In the ID-NPC topology, because the zero level is realized by independent components, although the switching loss is increased, the heat dissipation can be dispersed, and the switching frequency can be increased.

3. Three-Level and Two-Level Modulation Conversion Strategy Based on ID-NPC

3.1. I-TL (Improved Two-Level) Topology

The I-TL (improved two-level) topology is shown in Figure 11, and it is a part of the ID-NPC topology. Two groups of parallel switching elements are used on each bridge arm to improve the withstand voltage of the bridge arm. Two fast diodes are added to each bridge arm.

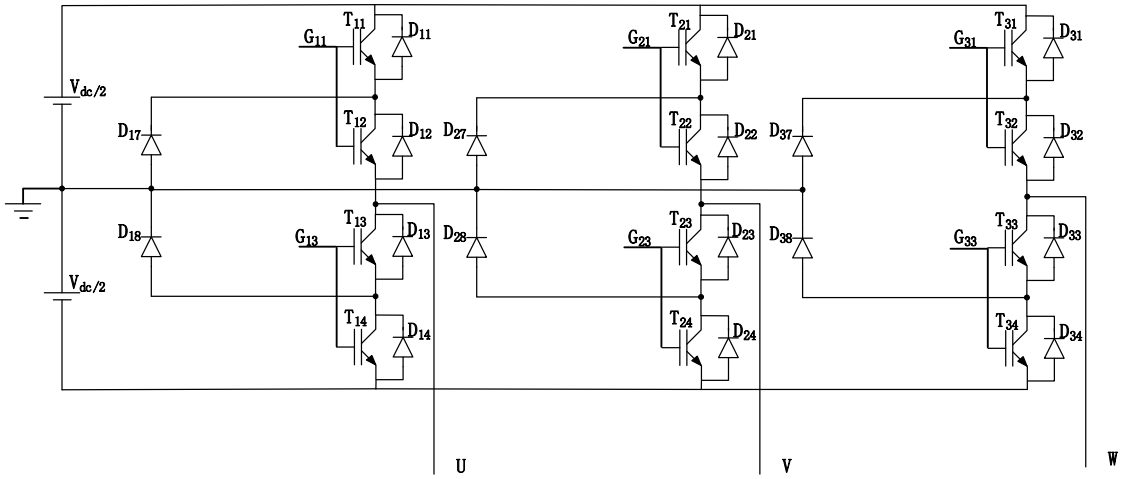

Figure 11. Improved two-level topology.

There is a reverse current in the UVW phase during shutdown, and, at the same time, the lower half of the bridge arm is opened, namely, the ("−1" "−1" "−1") state, G_{13}, G_{23}, and G_{33} are on, and the reverse current flows into the zero potential through T_{13} and D_{18}, T_{23} and D_{28}, and T_{33} and D_{38}, which increases the return path and reduces the impact of the reverse current on the on–off components.

3.2. Region Order Algorithm

The rotating voltage vector produces a rotating flux linkage, where the clockwise order is II → VI → IV→V → I → III, and the counterclockwise order is III → I → V → IV → VI → II. For a PMSM (permanent magnet synchronous motor), it is not very important which sector the rotation vector starts from, but it can rotate sequentially from this sector. For sector judgment, only the angle order is needed, and the sector number is just an identification of the order. The corresponding relationship is shown in Table 6.

Table 6. Corresponding relationship of sector, basic vector, αβ coordinate system region order, and RAM.

Sector	Basic Vector	αβ Coordinate System Region Order	RAM
III	T4, T6	$0-\pi/3$	1–683
I	T6, T2	$\pi/3-2\pi/3$	684–1366
V	T2, T3	$2\pi/3-3\pi/3$	1367–2048
IV	T3, T1	$3\pi/3-4\pi/3$	2049–2731
VI	T1, T5	$4\pi/3-5\pi/3$	2732–3414
II	T5, T4	$5\pi/3-6\pi/3$	3415–4096

3.3. Optimization of Vector Action Time

The SVPWM (space vector pulse width modulation) algorithm contains trigonometric function calculation; therefore, the calculation of the basic voltage vector action time is more complex. The vector action time is completely determined by U_1, U_2, and U_3, and some simple transformation can be conducted. Take the vector composition in the $(0-\pi/3)$ region as an example, as shown in Figure 12.

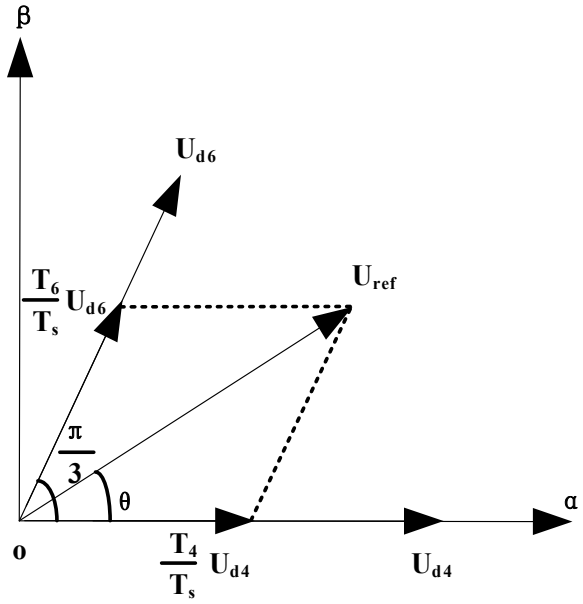

Figure 12. The vector composition in the $(0-\pi/3)$ region.

According to Figure 12 and the volt-second balance principle, we obtain the following formula:

$$\begin{cases} U_\alpha \times T_s = U_{ref} \times \cos\theta \times T_s = \frac{2}{3}U_d \times \cos 0 \times T_4 + \frac{2}{3}U_d \times \cos\frac{\pi}{3} \times T_6 \\ U_\beta \times T_s = U_{ref} \times \sin\theta \times T_s = \frac{2}{3}U_d \times \sin 0 \times T_4 + \frac{2}{3}U_d \times \sin\frac{\pi}{3} \times T_6 \end{cases}, \quad (1)$$

We can further launch

$$\begin{cases} T_4 = \frac{3U_\alpha \times T_s}{2U_d} - \frac{T_6}{2} = \frac{\sqrt{3}T_s}{U_d} \times \left(\frac{\sqrt{3}}{2}U_\alpha - \frac{1}{2}U_\beta\right) = \frac{\sqrt{3}T_s}{U_d} \times U_2 \\ T_6 = \frac{\sqrt{3}U_\beta \times T_s}{U_d} = \frac{\sqrt{3}T_s}{U_d} \times U_1 \\ T_0 = T_s - T_4 - T_6 \end{cases}, \quad (2)$$

Similarly, the time of each basic voltage vector in other regions can be obtained. According to U_1, U_2, and U_3, in Equation (2), the region of the reference voltage vector is determined. Then, by using the look-up table in the FPGA (field-programmable gate array), the action time of the basic voltage vector in the corresponding region can be obtained, and the relationship between the action time and the vector in the region is obtained, as shown in Table 7. In the table, $K = 1.732T_s/V_{dc}$, where V_{dc} represents the DC bus voltage.

Table 7. Relationship between the sector action time and the sector.

Order	T_i	T_j	T_0
$(0-\pi/3)$(T4, T6)	$T_4 = K \times U_2$	$T_6 = K \times U_1$	$T_0 = T_s - T_4 - T_6$
$(\pi/3-2\pi/3)$(T6, T2)	$T_6 = K \times -U_3$	$T_2 = K \times -U_2$	$T_0 = T_s - T_6 - T_2$
$(2\pi/3-3\pi/3)$(T2, T3)	$T_2 = K \times U_1$	$T_3 = K \times U_3$	$T_0 = T_s - T_2 - T_3$
$(3\pi/3-4\pi/3)$(T3, T1)	$T_3 = K \times -U_2$	$T_1 = K \times -U_1$	$T_0 = T_s - T_3 - T_1$
$(4\pi/3-5\pi/3)$(T1, T5)	$T_1 = K \times U_3$	$T_5 = K \times U_2$	$T_0 = T_s - T_1 - T_5$
$(5\pi/3-6\pi/3)$(T5, T4)	$T_4 = K \times U_1$	$T_4 = K \times U_2$	$T_0 = T_s - T_5 - T_4$

Due to U_1, U_2, U_3, and U_α, U_β is derived from $U_m\cos(\omega t)$ and $U_m\sin(\omega t)$. For PMSM, the rotation vector does not need to be judged on which sector it is located in but can rotate sequentially counterclockwise or clockwise. Therefore, the RAM allocation value is used to directly express the sector action time. Equation (3) can be obtained:

$$\begin{bmatrix} U_1 \\ U_2 \\ U_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} & -\frac{1}{2} \end{bmatrix} \times \begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = U_m \times \begin{bmatrix} 0 & 2 \\ 1 & -1 \\ -1 & -1 \end{bmatrix} \times \begin{bmatrix} 3\cdot\sqrt{\frac{1}{2}} \times \frac{1}{2} \times \cos(\omega t) \\ \sqrt{\frac{1}{2}} \times \frac{\sqrt{3}}{2} \times \sin(\omega t) \end{bmatrix} = \begin{bmatrix} 0 & 2 \\ 1 & -1 \\ -1 & -1 \end{bmatrix} \times \begin{bmatrix} C \\ D \end{bmatrix}, \quad (3)$$

$C = 3U_m \times (1/2)^{1/2} \times \cos(\omega t)/2 = 3U_m \times (1/2)^{1/2} \times A$ and $D = U_m \times (1/2)^{1/2} \times (3/4)^{1/2} \times \sin(\omega t) = U_m \times (1/2)^{1/2} \times B$ are stored in two 16-bit RAMs. The angle and action time are derived from Equation (2), and the relationship is shown in Table 8, $K = 1.732T_s/V_{dc}$.

Table 8. The relationship between angle and action time.

Order	T_i	T_j	T_0
RAM value	1–683	1–683	1–683
$(0-1/3\pi)$(T4, T6)	$T_4 = K \times (C-D)$	$T_6 = K \times 2C$	$T_0 = T_s - T_4 - T_6$
RAM value	684–1366	684–1366	684–1366
$(1/3\pi-2/3\pi)$(T6, T2)	$T_6 = K \times (C+D)$	$T_2 = K \times (D-C)$	$T_0 = T_s - T_6 - T_2$
RAM value	1367–2048	1367–2048	1367–2048
$(2/3\pi-3/3\pi)$(T2, T3)	$T_2 = K \times 2C$	$T_3 = K \times -(C+D)$	$T_0 = T_s - T_2 - T_3$
RAM value	2049–2731	2049–2731	2049–2731
$(3/3\pi-4/3\pi)$(T3, T1)	$T_3 = K \times (D-C)$	$T_1 = K \times -2C$	$T_0 = T_s - T_3 - T_1$
RAM value	2732–3414	2732–3414	2732–3414
$(4/3\pi-5/3\pi)$(T1, T5)	$T_1 = K \times -(C+D)$	$T_5 = K \times (C-D)$	$T_0 = T_s - T_1 - T_5$
RAM value	3415–4096	3415–4096	3415–4096
$(5/3\pi-6/3\pi)$(T5, T4)	$T_5 = K \times 2C$	$T_4 = K \times (C-D)$	$T_0 = T_s - T_5 - T_4$

3.4. Three–Two- and Two–Three-Level Modulation Conversion Strategy Based on Loss Allocation and Fault Tolerance

The number of winding phases is limited to three phases. Therefore, if one of the phase windings fails when a three-phase motor is driven by a D-NPC topology converter, the generated rotating magnetic field will be destroyed, inevitably leading to a difference between the winding currents of the other two phases without faults. In this case, a pulsed magnetic field will be generated, causing problems with the orientation of the rotor rotating magnetic field. In terms of the converter control system, the probability of a problem with the converter is greater than the probability of a problem with the motor winding, and the problem with a converter may easily expand to motor winding [20,21].

The improved ID-NPC increases the number of semiconductor switching elements and reduces the system economy. Moreover, the increase in the number of switching elements also brings about the decrease in the inherent reliability, but the increased switching elements can improve the heat loss distribution. When the neutral point potential balance is taken into account, the ID-NPC topology is composed of the positive level, negative level, and the independent zero level; therefore, it can work in the two-level state of the positive and negative levels, or in the three-level state of the positive, negative, and zero levels.

The short circuit and open circuit of switching elements are the main causes of converter fault. When only one is stuck open, the element shall be shorted or replaced. The two switching elements in the middle of the converter bridge arm of the traditional D-NPC topology are multiplexed elements, which suffer a higher fault probability and have a relatively short service life. If there is a short circuit between the two switching elements in the middle of the bridge arm, only one switching element remains in the part of the bridge arm where the short-circuit element is located, and when the other part of the bridge arm is turned on, the remaining switching element will withstand the full bus voltage, the breakdown probability will increase, and the entire bridge arm will be short-circuited.

In the ID-NPC topology, the upper positive and lower negative levels of the bridge arms are determined by two groups of parallel elements. When one of the two parallel elements in the bridge arm is short-circuited by a breakdown, or one element in the upper and lower parallel bridge arms is short-circuited by a breakdown, the converter can still operate in a three-level state.

In the ID-NPC topology, when one of the two parallel elements in the bridge arm is short-circuited by a breakdown, or one element in the upper and lower parallel bridge arms is short-circuited by a breakdown when the converter runs in the two-level state, it can still be in a two-level state.

Comparing with the traditional two-level converter, the D-NPC three-level converter has more conduction loss, and the switching loss is significantly reduced. When the switching frequency is higher (>10 Hz), the three-level topology converter has a higher conversion efficiency; therefore, a three–two-level modulation conversion strategy based on loss allocation and fault tolerance is proposed. When the driving frequency of PMSM is not greater than 10 Hz, the improved two-level SVPWM optimized modulation algorithm is adopted. When the frequency is greater than 10 Hz, the three-level SVPWM modulation algorithm is adopted. The conversion of the two modulation algorithms can help them complement each other to ensure that less heat is generated by loss and distributed uniformly, and that the neutral point potential deviation is controlled within the required range. The flowchart of modulation conversion is shown in Figure 13.

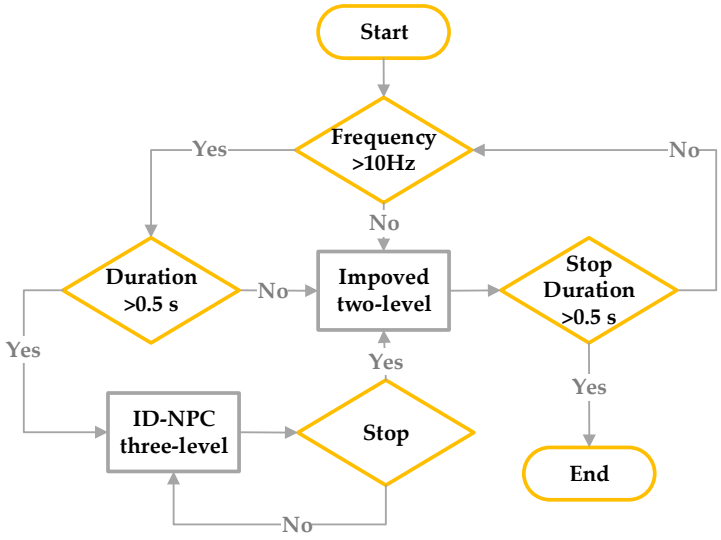

Figure 13. The flowchart of modulation conversion.

4. Simulation Analysis

4.1. Simulation Comparison Based on Two Two-Level Topologies

The simulation conditions are shown in Table 9.

Table 9. Simulation conditions.

Name	DC Voltage	Sampling Frequency	Simulation Time	Modulation Frequency
Value	30 V	10 kHz	1 s	48.8 Hz

The structures of the traditional two-level topology and the improved two-level topology based on ID-NPC are built. Under the same simulation conditions, the voltage waveforms are shown in Figure 14, where Uac1 and Ubc1 are the traditional two-level U_{ac} and U_{bc} voltage waveforms, respectively, and Uac2 and Ubc2 are the improved two-level U_{ac} and U_{bc} waveforms, respectively. Additionally, the x-axis is in seconds, and the y-axis is in volts.

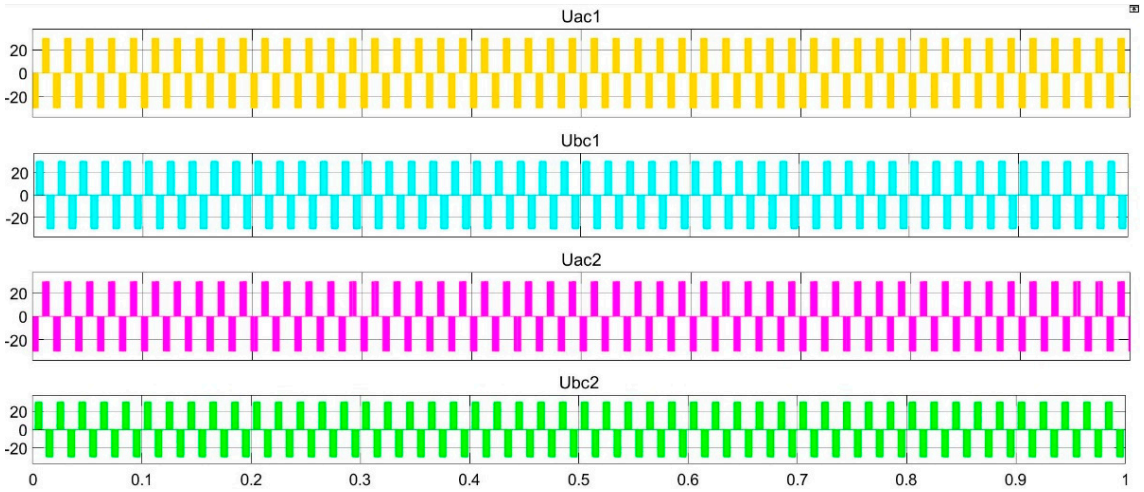

Figure 14. The simulation waveforms based on two topologies.

It can be seen from Figure 14 above that the simulation waveform based on the two topologies is basically the same, and this shows that the structure of the improved two-level topology has the same function as that of the traditional two-level topology.

4.2. Simulation Analysis of Three-Level and Two-Level Modulation Conversion Strategies

Figure 15 is the simulation voltage waveform of three–two-level modulation conversion, and Figure 16 is the simulation voltage waveform of two–three-level modulation conversion. The units of U_{ac} and U_{bc} are in volts. The simulation time is one second, and when the time is at 0.5 s, the level converts from three-level to two level or two-level to three-level. It can be seen from the below two figures that the voltage fluctuation is small, which indicates that the conversion influence is relatively small.

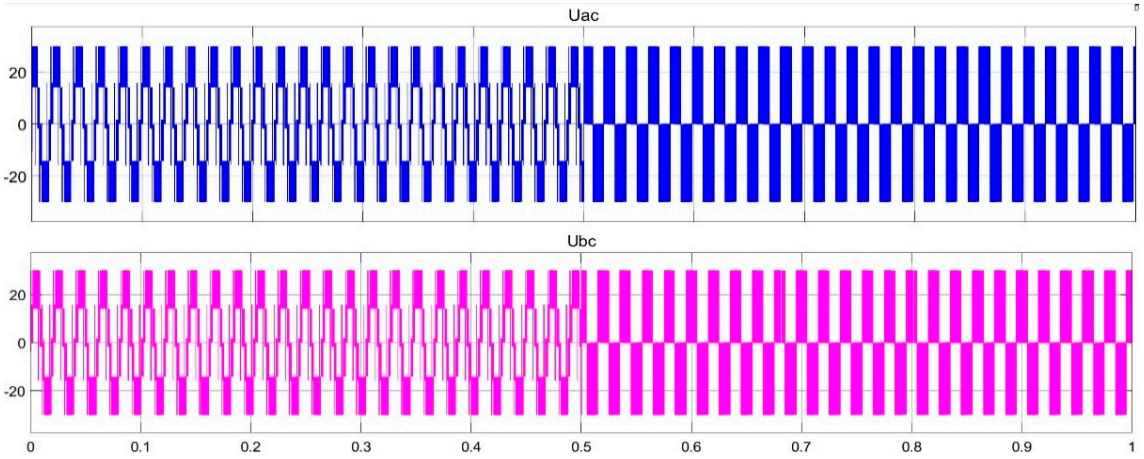

Figure 15. The simulation voltage waveform of three–two-level modulation conversion.

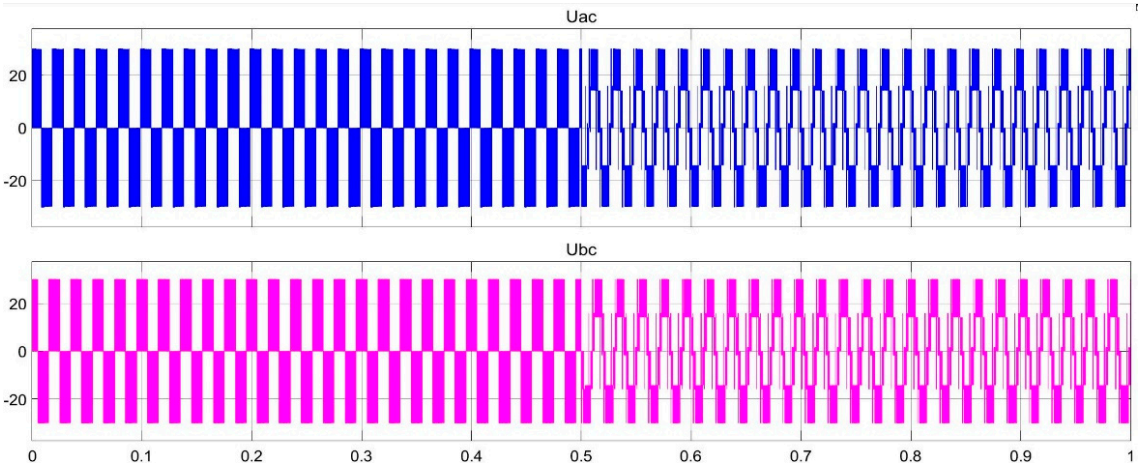

Figure 16. The simulation voltage waveform of two–three-level modulation conversion.

Using a two-level start, a three-level operation, and a two-level stop, the U_{ac} and U_{bc} simulation waveforms of the whole process are shown in Figure 17. The simulation time is 1.5 s. At 0.5 s, two-level (6.1 Hz) converts to three-level (48.8 Hz), and at 1.0 s, three-level (48.8 Hz) converts to two-level (6.1 Hz) until it stops. The feasibility of the three-level and two-level modulation conversion strategies based on loss allocation and fault tolerance is verified. The units of U_{ac} and U_{bc} are in volts.

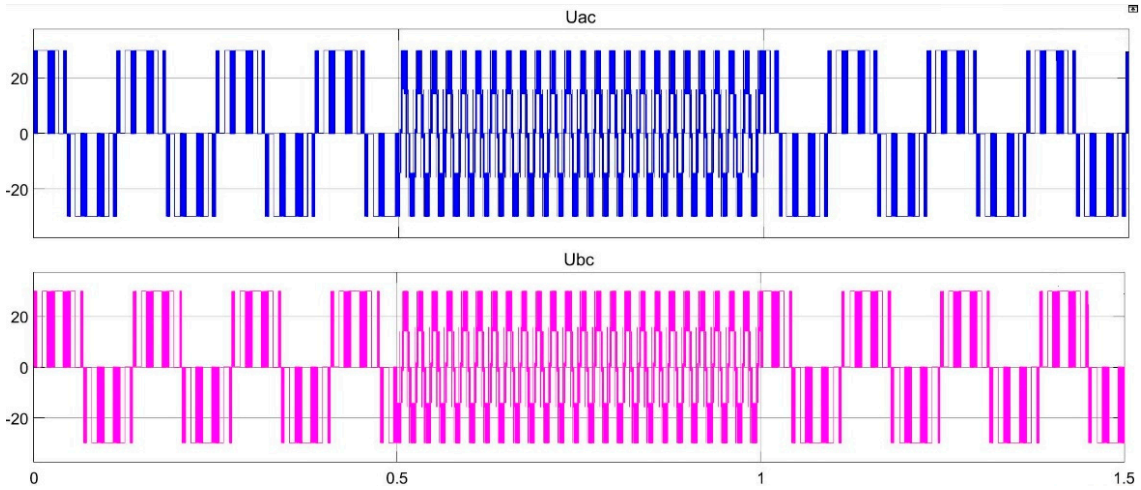

Figure 17. The simulation voltage waveform of the whole conversion process.

5. Experimental Analysis

5.1. Experimental Comparison Based on Two Two-Level Topologies

The experimental parameters are consistent with the above simulation parameters, and the voltage waveforms are shown in Figure 18, where 1 and 2 are the traditional two-level U_{ac} and U_{bc} voltage waveforms, respectively, and 3 and 4 are the improved two-level U_{ac} and U_{bc} waveforms, respectively. The experimental waveform is basically consistent with the simulation waveform.

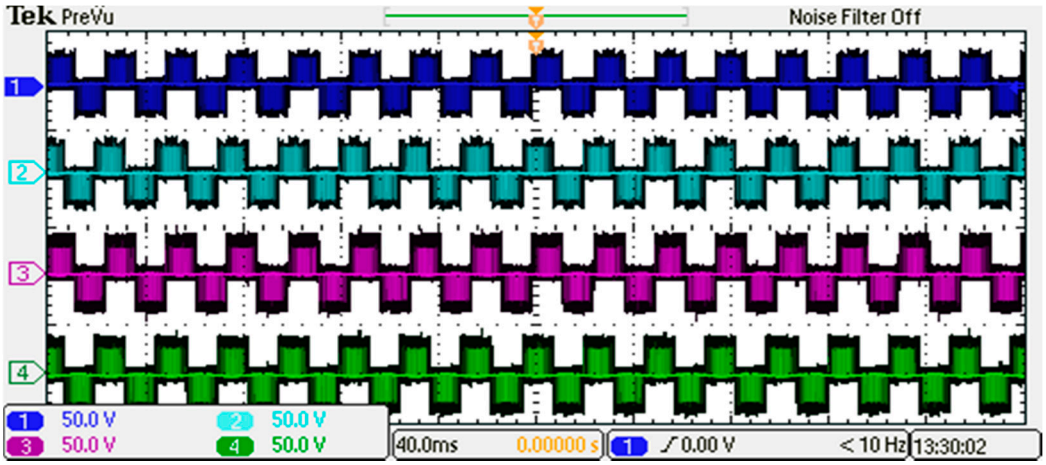

Figure 18. The experimental waveforms of two topologies.

5.2. Experimental Analysis of Three-Level and Two-Level Modulation Conversion Strategies

The experimental waveform of three–two-level modulation conversion is shown in Figure 19. The experimental waveform of two–three-level modulation conversion is shown in Figure 20. The whole conversion process of the modulation strategy is shown in Figure 21. In those figures, 1 is the U_{ac} voltage waveform, and 2 is the U_{bc} waveform.

By comparing the conversion results of the three–two-level and two–three-level experiments, it can be seen from the figures that the experimental waveform reflects the simulation waveform, and the difference in waveforms has a relationship with the sampling time in the process of simulations and experiments.

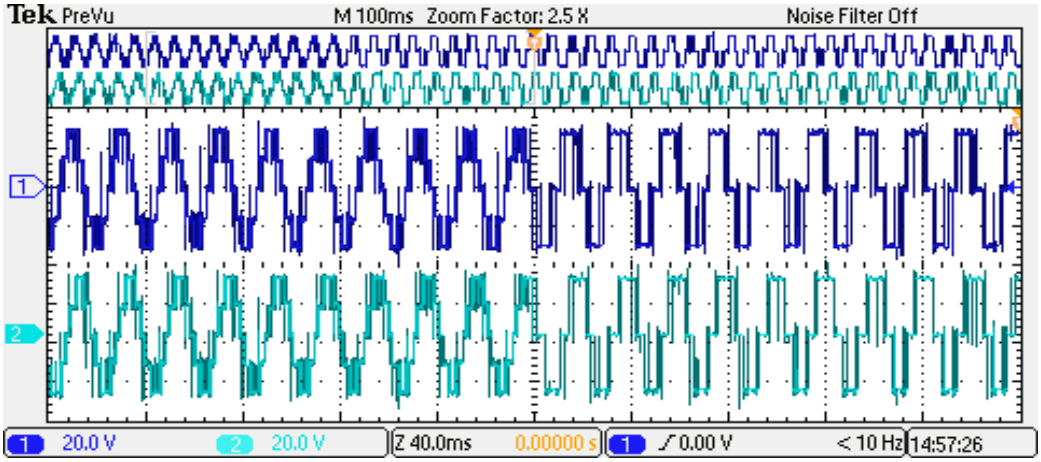

Figure 19. The experimental waveform of three–two-level modulation conversion.

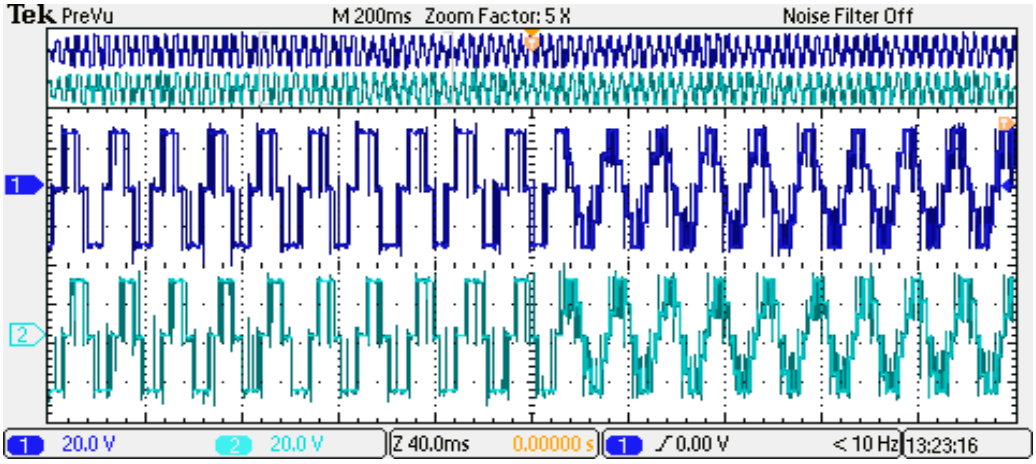

Figure 20. The experimental waveform of two–three-level modulation conversion.

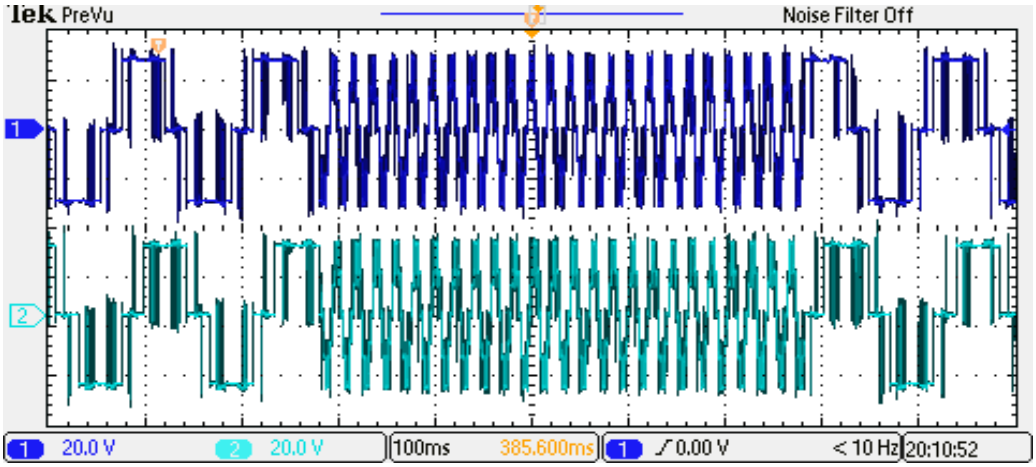

Figure 21. The whole conversion process of the modulation strategy.

6. Summary

The switching losses of the D-NPC and ID-NPC topologies were qualitatively compared and analyzed. In the ID-NPC topology, 18 IGBTs can make the heat distribution more uniform and prolong the service life of all IGBTs. Additionally, the circuit of the

ID-NPC topology can also save three groups of driving elements. The improved two-level topology was used, where, on the one hand, the current return path was added and, on the other hand, the three-level and two-level conversion strategies were adopted to expand the fault-tolerant function of the system, and to improve the reliability. The simulation and experiment further verify the function integrity of the improved topology and the feasibility of the modulation conversion strategy.

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