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Multi-Layer QCA Reversible Full Adder-Subtractor Using Reversible Gates for Reliable Information Transfer and Minimal Power Dissipation on Universal Quantum Computer

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Abstract: The effects of quantum mechanics dominate nanoscale devices, where Moore's law no longer holds true. Additionally, with the recent rapid development of quantum computers, the development of reversible gates to overcome the problems of energy and information loss and the nano-level quantum-dot cellular automata (QCA) technology to efficiently implement them are in the spotlight. In this study, a full adder-subtractor, a core operation of the arithmetic and logic unit (ALU), the most important hardware device in computer operations, is implemented as a circuit capable of reversible operation using QCA-based reversible gates. The proposed circuit consists of one reversible QCA gate and two Feynman gates and is designed as a multi-layer structure for efficient use of area and minimization of delay. The proposed circuit is tested on QCADesigner 2.0.3 and QCADesigner-E 2.2 and shows the best performance and lowest energy dissipation. In particular, it shows tremendous improvement rates of 180% and 562% in two representative standard design cost indicators compared to the best existing studies, and also shows the highest circuit average output polarization.

Keywords: reversible computing; quantum-dot cellular automata; reversible full adder-subtractor; reversible gate; power dissipation; universal quantum computer

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1. Introduction

The International Technology and Roadmap for Semiconductors (ITRS) points out major problems with existing CMOS technology, such as high-power loss, threshold voltages, thermal runaway, and high leakage current, and states that it is approaching the end of its semiconductor nano-system roadmap [1]. Moore's law, which states that the number of components on a single chip doubles approximately every two years [2], no longer applies in nanoscale devices, and various quantum mechanical effects dominate device physics [3]. In addition, as CMOS-VLSI micro technology reduces the size of transistors disproportionately, large energy and information losses are emerging as major problems. Information loss is a major problem in irreversible digital computation systems, and there is a large and growing demand for nanoscale computation systems that can minimize heat dissipation [4].

Therefore, the design of reversible circuits is a key structural engineering challenge for solving the problem of information loss while minimizing energy dissipation. Landauer demonstrated that 1-bit information loss results in energy dissipation of $k_B T \ln 2$ joules, where $k_B = 1.38 \times 10^{-23}$ JK^{-1} is the Boltzmann constant and T is the temperature in Kelvin [5]. At room temperature (T = 300 K), the heat release occurring during a binary transaction is 0.017 eV and is considered physically irreversible, and this microscopic physical state can be restored to what it was before the process occurred. Bennett demonstrated the validity that energy loss of $k_B T \ln 2$ joules in an irreversible circuit can be recovered in a reversible circuit [6].

Recently, with the rapid rise of quantum computing [7], quantum logic gates are attracting attention as logic gates that can replace existing digital circuits in quantum circuit calculation models. The Toffoli gate, developed in 1980, is a universal gate that can implement any desired Boolean function as a reversible circuit [8], and it can be realized by five two-qubit quantum gates [9]. Along with this, various universal reversible gates, such as the Fredkin gate, Feynman gate, and Peres, were developed [10–12]. Since then, various reversible gates, such as RUG [13], RQCA [14], URG [15], TR [16], and PQR [17], have been continuously developed and implemented using QCA [18].

Quantum-dot cellular automata (QCA), proposed by Lent and Tougaw, has emerged as an alternative to overcome the problems of existing CMOS and implements existing reversible circuits with ultra-low power consumption. The dissipated energy is measured based on the Hamiltonian matrix, using the HartreeFock approximation in relation to the Coulomb repulsion between QCA cells, as shown in (1) [19].

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i C_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}\left(C_{j-1} + C_{j+1}\right) & -\gamma \\ -\gamma & \frac{E_k}{2}\left(C_{j-1} + C_{j+1}\right) \end{bmatrix} \quad (1)$$

where E_k is the energy cost of two neighboring cells with opposite polarization, called kink energy, C_i denotes the polarization of the i-th neighboring cell, and $f_{i,j}$ denotes the geometrical factor identifying the electrostatic interaction between cells i and j due to the geometrical distance. This kink energy is related to the energy cost of two cells with the opposite polarization. γ denotes the electron tunneling energy inside the cell, which is controlled by the clock. The nonadiabatic power estimation model was used to estimate the power loss or energy dissipation of the cell [20,21]. The expected value of the Hamiltonian at each time instant is given by

$$E = \langle H \rangle = \frac{\hbar}{2}\vec{\Gamma}\cdot\vec{\lambda} \quad (2)$$

where $\vec{\Gamma}$ is the 3-D energy vector, and $\vec{\lambda}$ is the coherence vector. Based on (2), the equation for instantaneous power is given as (3).

$$P_{Total} = \frac{dE}{dt} = \frac{\hbar}{2}\left(\frac{d\vec{\Gamma}}{dt}\right)\cdot\vec{\lambda} + \frac{\hbar}{2}\vec{\Gamma}\cdot\left(\frac{d}{dt}\vec{\lambda}\right) \quad (3)$$

The first term in (4) represents the power going in and out of the clock and inter-cell power flow, and the second term represents the power dissipated. By multiplying these two terms, the power dissipation at a specific time can be obtained.

$$P_{diss}(t) = \frac{\hbar}{2}\vec{\Gamma}(t)\cdot\left(\frac{d}{dt}\vec{\lambda}(t)\right) \quad (4)$$

Therefore, power dissipation can be summarized in terms of energy per clock cycle, as shown in (5).

$$P_{diss} = \frac{E_{diss}}{T_c}\left\langle \frac{\hbar}{2T_c}\vec{\Gamma}_+ \times \left[-\frac{\vec{\Gamma}_+}{\left|\vec{\Gamma}_+\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_+\right|}{k_B T}\right) + \frac{\vec{\Gamma}_-}{\left|\vec{\Gamma}_-\right|}\tanh\left(\frac{\hbar\left|\vec{\Gamma}_-\right|}{k_B T}\right)\right]\right\rangle \quad (5)$$

where T_c is the clock period and $\vec{\Gamma}_+$ and $\vec{\Gamma}_-$ are the Hamiltonian values before and after the transaction processing.

Multilayer structures are a design method that minimizes energy dissipation and are a field of QCA design that is being studied extensively. Although feasibility is lower and design cost is higher than that of a co-planar structure, a well-designed multi-layer structure plays a significant role in minimizing space, delay, and energy consumption, and is continuously being studied at various major universities and research institutes.

In 2020, Song et al. [22] and Heikalabad et al. [23] proposed a QCA-based RAM and full adder using a multi-layer structure, respectively, and in 2021, Chu et al. proposed a 3-input XOR-based QCA BCD adder using a multi-layer structure [24]. In 2022, Perri et al. [25] and Das et al. [26] proposed a QCA multi-bit comparator and a 3:8 decoder using a multi-layer crossover, respectively.

In 2023 and 2024, Khan et al. presented various analyses of the latest trends and problems related to QCA design [27,28]. In particular, much research has been conducted based on QCA on the full adder-subtractor (FAS), the core circuit of the ALU, which consumes the most power in computer processors [29–31], and research on reversible FAS (RFAS) continues to minimize energy dissipation. Recently, various reversible gates have been implemented using QCA.

Kianpour et al. designed a Toffoli gate and a Fredkin gate using a rotated QCA cell and proposed RFAS based on a QR gate using these gates [32]. Hashemi et al. and Kumar et al. proposed RFA without a subtractor along with a new reversible gate using a QCA-based 3-input majority gate and a 5-input majority gate, respectively [33,34]. Taherkhani et al. proposed a more efficient RFAS using the newly proposed reversible QCA gate (RQG) and two Feynman gates (FGs) [35], and Ahmad et al. developed a new reversible gate (NRG) using QCA-based multiple gates and FG, and proposed NRG-based RFAS [36]. Vahabi efficiently redesigned various reversible gates using QCA and proposed RFAS with excellent performance using the existing RQG [37]. Table 1 summarizes the major contributions to the development of RFA(S).

Table 1. Major contributions to the development of RFA(S).

Reference	Year	Structure	Major Contributions
[32]	2017	RFAS	3 × 3 QCA Reversible (QR) gate using Toffoli and Fredkin gates
[33]	2018	RFA	4 × 4 N1 and 3 × 3 N2 gates based on a 5-input majority gate
[34]	2019	RFA	Area optimization using a 5-input majority gate
[35]	2017	RFAS	3 × 3 Reversible Quantum Gate (RQG)
[36]	2018	RFAS	3 × 3-New Reversible Gate (NRG) and Modified Feynman Gate (MFG)
[37]	2023	RFAS	Optimization of RQG

In this study, we review previously proposed QCA-based RFAS circuits and propose the most efficient RFAS that improves the problems of the circuits using QCA. The contributions of this study are summarized as follows.

- Review of the structure, operation, and characteristics of existing excellent QCA-based RFAS circuits
- Design of a reversible quantum gate (RQG)-based RFAS after presenting the problems of implementing the existing QCA circuits
- Best performance in all aspects compared with the existing circuits and significant improvements of at least 67% and 54% in delay and energy dissipation, respectively.
- Remarkable improvements of 180% and 562% in two representative design costs, $Cost_{AD}$ and $Cost_{ED}$, respectively, compared to the best existing circuit
- Noise-free and high and stable output polarization, especially a significant improvement of 3.8% in the average output polarization
- Proposal of an efficient QCA-based RFAS that minimizes information loss and provides reliable information transmission through the best performance of the proposed reversible circuit

The structure of the paper is as follows. Section 2 explains the basic operation principle of QCA and reviews existing QCA reversible full adder-subtractors. Section 3 explains the operation and structure of the proposed reversible full adder-subtractor. Section 4 analyzes and compares the results through simulations. Section 5 concludes.

2. Related Works

In this section, we look at basic gate operations and clock states using QCA, and review existing reversible gates and RFAS circuits based on them. Various reversible gates are being developed to optimize RFAS, but there are still many shortcomings in areas, delays, energy dissipation, and output polarization.

2.1. QCA Gates and Clock Sates

A QCA cell consists of four quantum dots and is located at each corner of a square. Two electrons repel each other by Coulomb repulsion and exist in two quantum dots located diagonally among the four quantum dots. There are two such cases, and each polarization is expressed as $P = +1$ or $P = -1$, and in binary operation, they correspond to "1" and "0", respectively [38,39]. Logical operations in the QCA environment are based on a majority vote function in which the result value is the value of two or more of the three inputs and are implemented through a majority gate in the QCA environment. Figure 1a,d show a majority gate and a rotated majority gate with three inputs A, B, and C, respectively. If the polarization of one of these inputs is fixed to $P = +1$ or $P = -1$, it is used as a 2-input AND and OR logic gate, respectively, as shown in Figure 1b,c. Another representative logical operation is an Inverter. Figure 1e is a robust NOT gate that makes the output signal stronger, and Figure 1f is a simple NOT gate that can be easily implemented in a small space [40,41].

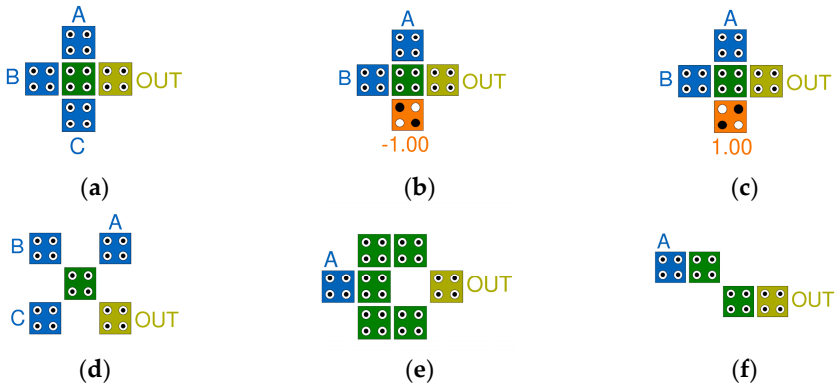


Figure 1. QCA logic gates: (**a**) 3-input majority gate; (**b**) AND gate; (**c**) OR gate; (**d**) rotated 3-input majority gate; (**e**) robust NOT gate; (**f**) simple NOT gate.

A QCA cell has four clock states, and the circuit operates by repeating changes from clock0 to clock3 [19,39]. The switch state refers to a state in which the barrier between quantum dots gradually increases as the potential energy of electrons becomes stronger. In the hold state, the potential energy of electrons becomes high enough to prevent them from crossing the barrier between quantum dots. At this time, each cell has a clear polarization and the strongest potential energy. In the release state, electrons gradually lose potential energy, and the barrier between quantum dots gradually decreases. In the relaxed state, the potential energy of the electrons is lowered so that they can freely pass through the barrier between quantum dots, and the cell does not have any polarization. Figure 2 shows a graph of the barrier height and time relationship between quantum dots according to the four states of the QCA cell.

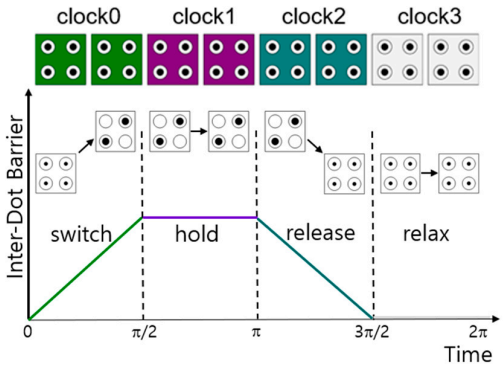


Figure 2. Four states of the QCA clock.

2.2. Conventional QCA Reversible Full Adder-Subtractors

Recently, various reversible gates have been proposed, and efficient RFAS using them are being proposed. As shown in the truth table in Table 2, RFAS has three inputs, A, B, and C, and three outputs, Carry, Borrow, and Sum/Diff. It can also have additional garbage inputs and outputs to enable reversible operations. To obtain the output Carry, Borrow, and Sum/Diff, the operation of $MG(A, B, C)$, $MG(A\prime, B, C)$, and $A \oplus B \oplus C$ were used respectively.

Table 2. Truth table of RFAS.

Inputs			Outputs		
A	**B**	**C**	**Carry**	**Borrow**	**Sum/Diff**
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	1	1	1

Figure 3 shows the logic diagram of the reversible full adder circuit proposed by Hashemi et al. [33]. They newly proposed two reversible gates, 4 × 4 N1 and 3 × 3 N2. The N1 gate uses a 3-input majority gate to output Carry, and the N2 gate uses a 5-input majority gate to output two garbage values and Sum.

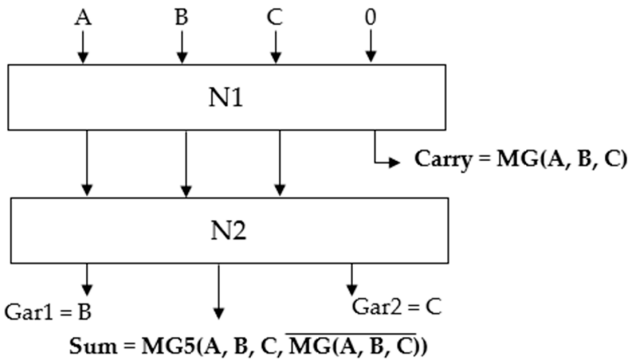


Figure 3. Logic diagram of RFA proposed by Hashemi et al. [33].

Taherkhani et al. developed a 3 × 3 RQG producing three outputs, $MG(A, B, C)$, $MG(A\prime, B, C)$, and $A \oplus B \oplus C$, and proposed an RFAS circuit with two FGs [35]. The first

FG was used to match the number of inputs and outputs for a reversible operation, and the second FG was used for an additional reversible XOR operation. Figure 4 shows the logic diagram of RFAS proposed by Taherkhani et al.

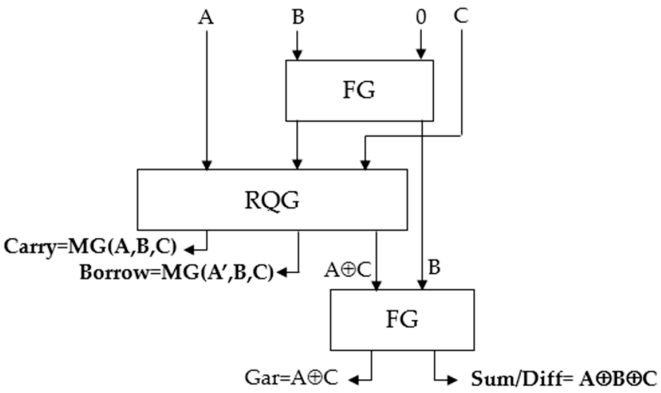


Figure 4. Logic diagram of RFAS proposed by Taherkhani et al. [35].

Ahmad et al. proposed a single-layer RFSA with 3 × 3 NRG and 2 × 2 MFG [36], as shown in Figure 5. The three inputs, A, B, and C, each pass through two MGs to produce output values Carry and Borrow. The MFG plays the same role as the FG and passes through two MFGs to output Sum/Diff, which is the output value of the full adder-subtractor.

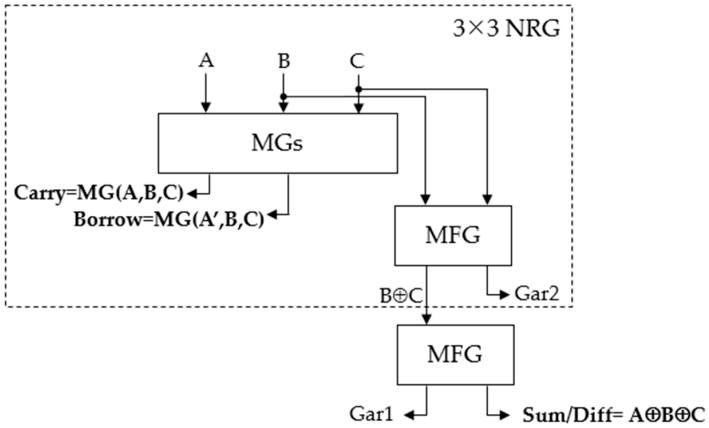


Figure 5. Logic diagram of RFAS proposed by Ahmad et al. [36].

Vahabi et al. recently proposed a circuit that improved the performance of RFAS using existing RQG. In the existing circuit, an attempt was made to minimize the overall area and delay by excluding the first FG and using a new XOR gate [37], as shown in Figure 6. However, because the number of inputs and outputs is different, it cannot function as a logical or physical reversible circuit.

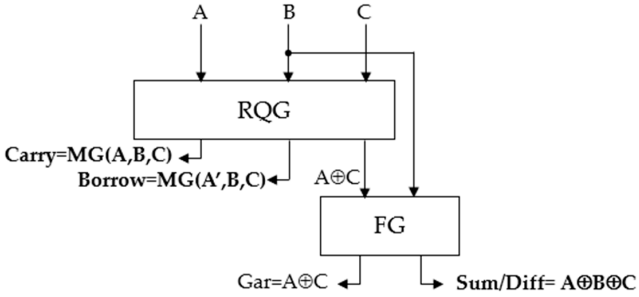
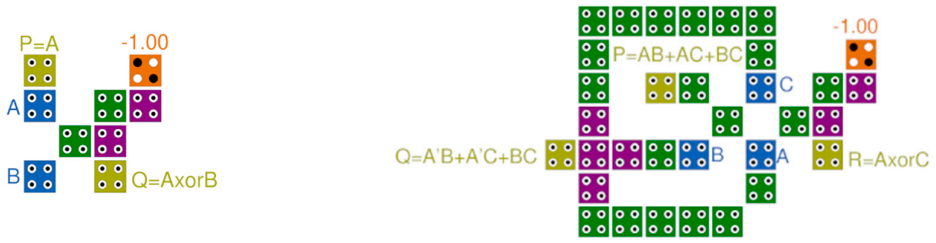


Figure 6. Logic diagram of RFAS proposed by Ahmad et al. [37].

3. Proposed Reversible Full Adder-Subtractor

This section shows the RFAS circuit proposed in this study. To effectively implement the proposed circuit, the 3-input XOR gate proposed in paper [42] is modified to a 2-input XOR gate. In addition, we implement the logic diagram of reversible RFAS based on RQG introduced in Figure 4. For this purpose, the QCA implementation of effective FG and RQG circuits is necessary.

Figure 7a implements the 2 × 2 FG using the proposed 2-input XOR gate using QCA. It has two inputs, A and B, and two outputs, P and Q. The value input to A can be directly output as the value of P, and the value of Q is output by the XOR operation of A and B. Figure 7b shows the QCA layout of RQG using one majority gate, one rotated majority gate, and the proposed 2-input XOR gate. At the center of the circuit is a rotated majority gate consisting of three inputs, A, B, and C, which produces the first result, P. A has the value A' by the simple inverter located at the bottom, and the remaining inputs, B and C, meet at the majority gate located on the left side of the circuit to produce Q. At the same time, A and C produce the value of R by operating with the 2-input XOR gate located on the right side of the circuit.



(**a**) (**b**)

Figure 7. Proposed QCA implementation of reversible gates: (**a**) FG; (**b**) RQG.

Figure 8 shows the QCA layout of the proposed multi-layered 4 × 4 RFAS circuit consisting of three layers. The first layer, as shown in Figure 8b, faithfully implements the RQG circuit shown in Figure 7b. Two FGs are implemented in the third layer of Figure 8d. Figure 8c serves as a bridge connecting the first and third layers. In the first clock phase, the input value B of the third layer crosses the bridge of the second layer and comes down to the first layer. In the second phase, the FG located on the left side of the circuit of the third layer outputs B as inputs of B and D, and transmits it to the input value of the FG on the right side of the circuit. At this time, the value of the A⊕C output from the first layer is transmitted to the input of the FG of the third layer through the bridge of the second layer, and Carry and Borrow are also output. Finally, in the third phase, Sum/Diff is output through the XOR operation on the two values input to FG.

Figure 9 shows the simulation results of the proposed RFAS. In Figure 9, it is confirmed that Carry and Borrow are output on CLOCK1, the second clock phase, and Sum/Diff are output on CLOCK2, the third clock phase. In addition, the RFAS circuit outputs normally, as shown in Table 2, and the output polarization is very high, up to 0.992, and a stable output signal without noise is confirmed. The following metrics are defined for performance comparison. Cell count refers to the number of cells required for circuit design, area refers to the rectangular area required for circuit design, and delay refers to the clock cycle (1 clock cycle = 4 clock phases) until the first output of the circuit is produced.

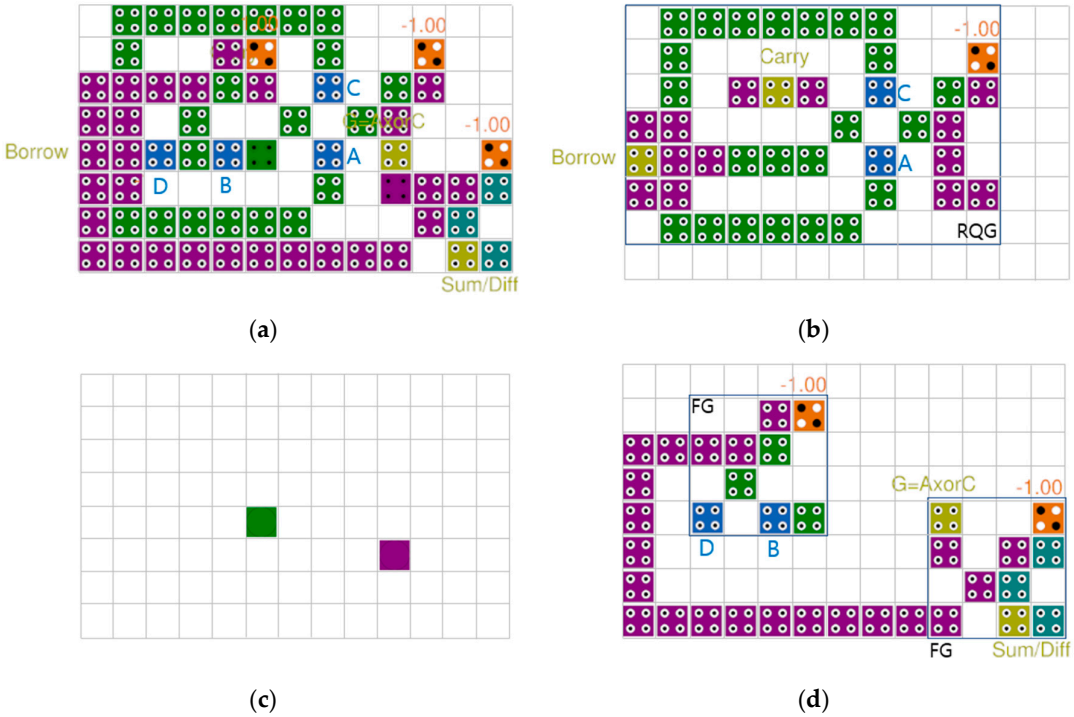


Figure 8. QCA implementation of the proposed RFAS: (**a**) top view; (**b**) first layer; (**c**) second layer; (**d**) third layer.

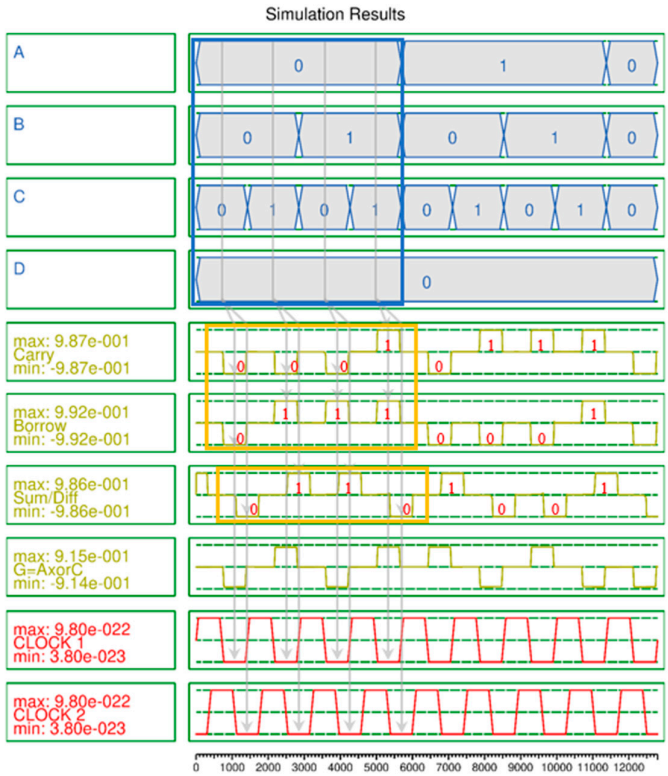


Figure 9. Simulation results of the proposed RFAS circuit.

4. Simulation and Performance Analysis

In this section, QCADesigner 2.0.3 and its extended version, QCADesigner-E 2.2, are used to measure QCA performance and energy dissipation [43,44]. They each use

"Bistable Approximation" and "Coherence Vector with Energy" as simulation engines, and the related parameters are summarized in Table 3.

Table 3. Simulation engines and parameters.

	QCADesigner 2.0.3	QCADesigner-E 2.2
Parameters	**Bistable Approximation**	**Coherence Vector with Energy**
Cell size (nm)	18	18
Dot diameter (nm)	5	5
Cell separation (nm)	2	2
Layer separation (nm)	11.5	11.5
Clock high (J)	9.8×10^{-22}	9.8×10^{-22}
Clock low (J)	3.8×10^{-23}	3.8×10^{-23}
Clock shift	0	0
Clock amplitude factor	2.0	2.0
Relative permittivity	12.9	12.9
Radius of effect (nm)	65	80
Number of samples	12,800	-
Convergence tolerance	1.0×10^{-3}	-
Maximum iterations per sample	100	-
Temperature (K)	-	1
Relaxation time (s)	-	1.0×10^{-15}
Clock slope (s)	-	1.0×10^{-12}
Time step (s)	-	1.0×10^{-16}
Clock/input period (s)	-	4.0×10^{-12}

Recently, with the rapid development of hardware, the importance of delay is evaluated more highly than area. Therefore, Equation (7) is the most commonly used cost calculation formula including area and delay [45,46]. Here, area and delay refer to the rectangular area and clock phase required for circuit design, respectively. In particular, the area of a multi-layer structure is the flat area multiplied by the number of layers. Equation (6) is applied to the area of a multilayer structure.

$$Area_{multi-layer} = Area_{single-layer} \times m \tag{6}$$

where m is the number of layers on a multi-layer structure to reflect the higher area cost of a multi-layer design over a coplanar structure [24,45].

As shown in Table 4, the proposed circuit performs both reversible full adder and full subtractor, and has the best performance and cost in terms of number of cells, area, delay, and $Cost_{AD}$. Compared to the best existing structure in [37], it showed significant improvements of 67% and 180% in delay and $Cost_{AD}$. Due to the rapid development of hardware, delay is becoming more important than area, so $Cost_{AD}$ is proportional to the square of delay.

$$Cost_{AD} = A \times D^2 \tag{7}$$

where A and D refers to the area and the delay of a circuit, respectively. Equation (8) is a standard design cost measurement method including energy dissipation and delay [44,45]. The importance of energy dissipation is viewed as being equal to delay, and $Cost_{ED}$ is proportional to the square of energy dissipation and the square of delay.

$$Cost_{ED} = E^2 \times D^2 \tag{8}$$

where E and D refers to the energy dissipation and the delay of a circuit, respectively [47]. Avg_Ebath and Sum_Ebath in Table 5 indicate the average energy dissipation per cycle and the total energy dissipation for all coordinates, respectively [48–51]. Both Avg_Ebath and

Sum_Ebath showed an improvement of 54% compared to the existing circuit in [37], which had the lowest energy dissipation, and $Cost_{ED}$ achieved a remarkable reduction of 562%.

$$\text{AOP} = \sum_{1}^{n} \frac{\text{Max Polarization} - \text{Min Polarization}}{2n} \quad (9)$$

Table 4. Performance comparison of RFA(S) circuits.

Circuit	Cell Count		Area		Delay		$Cost_{AD}$		Operation
	no.	Ratio	μm^2	Ratio	Clock	Ratio	AD^2	Ratio	
[32]	399	5.18	0.50	4.2	2	2.67	2.00	29.6	RFAS
[33]	236	3.06	0.32	2.7	3.25	4.33	3.38	50.1	RFA
[34]	178	2.31	0.23	1.9	3.25	4.33	2.43	36.0	RFA
[35]	228	2.96	0.28	2.3	1.75	2.33	0.86	12.7	RFAS
[36]	121	1.57	0.14	1.2	1.25	1.67	0.22	3.2	RFAS
[37]	123	1.60	0.12	1.0	1.25	1.67	0.19	2.8	RFAS
Ours	77	1.00	0.12	1.0	0.75	1.00	0.07	1.0	RFAS

Table 5. Energy dissipations and $Cost_{ED}$ comparison of RFA(S) circuits.

Circuit	Avg_Ebath		Error_Avg		Sum_Ebath		Error_Sum		$Cost_{ED}$	
	10^{-3} eV	Ratio	-10^{-4} eV	Ratio	10^{-2} eV	Ratio	-10^{-3} eV	Ratio	E^2D^2	Ratio
[33]	5.39	2.74	4.21	2.52	5.93	2.73	4.63	2.52	371.43	140.23
[34]	4.90	2.49	3.95	2.37	5.38	2.48	4.35	2.36	305.73	115.42
[35]	4.66	2.37	3.45	2.07	5.13	2.36	3.79	2.06	80.60	30.43
[36]	3.52	1.79	3.01	1.80	3.87	1.78	3.31	1.80	23.40	8.83
[37]	3.04	1.54	2.49	1.49	3.35	1.54	2.74	1.49	17.54	6.62
Ours	1.97	1.00	1.67	1.00	2.17	1.00	1.84	1.00	2.65	1.00

The average output polarization (AOP) is an important indicator of the output strength of a circuit [48]. The output of a circuit with high AOP can stably transmit values to subsequent circuits, so it is one of the important performance indicators that is directly related to the scalability and connectivity of the circuit. AOP calculates the average of the highest and lowest values of output polarization, as shown in Equation (9) [52]. As shown in Table 6, the highest meaningful AOP of the proposed circuit was measured at all outputs. The total AOP, calculated as the average value of AOP of all outputs, improved by more than 3.8% compared to the best existing circuit in [37].

Table 6. Average output polarization of RFA(S) circuits.

Circuit	Carry		Borrow		Sum/Diff		Total	
	AOP	Ratio	AOP	Ratio	AOP	Ratio	AOP	Ratio
[33]	9.540	0.967	-	-	9.550	0.969	9.545	0.966
[34]	9.540	0.967	-	-	9.550	0.969	9.545	0.966
[35]	9.540	0.967	9.550	0.963	9.540	0.968	9.543	0.966
[36]	9.540	0.967	9.530	0.961	9.530	0.967	9.533	0.965
[37]	9.540	0.967	9.530	0.961	9.475	0.961	9.515	0.963
Ours	9.870	1.000	9.920	1.000	9.860	1.000	9.883	1.000

5. Conclusions

Recently, due to the development of quantum computers, much attention has been paid to the development and implementation of reversible gates. This is because effective implementation of reversible gates can accelerate the development of universal quantum

computers and dramatically improve the performance of computing systems by minimizing energy and information loss. The proposed study constructed a FAS, one of the operation circuits that has the greatest impact on the performance of computing systems, as a circuit capable of reversible operation using QCA-based reversible gates. Although there have been QCA implementations for circuit design using various existing reversible gates, the RFAS using multilayer RQG proposed in this study was verified to be the best in all performance aspects such as area, delay, energy dissipation, and AOP required for circuit design. In addition, it demonstrated outstanding excellence in two standard design cost indicators compared to existing excellent circuits. The implementation of RFAS and reversible gates using multi-layer QCA can lead to many creative ideas and development of various circuits. However, it always has a weakness in the difficulty of actual implementation. With the rapid development of 3D stacked memories such as HBM in semiconductors, the feasibility of multilayer structures in QCA is increasing, and QCA technology will further develop through challenging research.

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