

Article

A 250 °C Low-Power, Low-Temperature-Drift Offset Chopper-Stabilized Operational Amplifier with an SC Notch Filter for High-Temperature Applications

Zhong Yang ^{1,2}, Jiaqi Li ^{1,2}, Jiangduo Fu ^{1,2}, Jiayin Song ^{1,2}, Qingsong Cai ^{1,2} and Shushan Qiao ^{1,2,*}

¹ Institute of Microelectronics of the Chinese Academy of Sciences, Chaoyang, Beijing 100029, China; yangzhong13@mailsucas.ac.cn (Z.Y.); lijiaqi_hn@163.com (J.L.); fujiangduo20@mailsucas.ac.cn (J.F.); songjiayin@ime.ac.cn (J.S.); qingsongcai9@163.com (Q.C.)

² University of Chinese Academy of Sciences, Shijingshan, Beijing 100049, China

* Correspondence: qiaoshushan@ime.ac.cn

Abstract: This paper proposes a three-stage op amp based on the SOI (silicon-on-insulator) process, which achieves a low offset voltage and temperature coefficient across a wide temperature range from $-40\text{ }^{\circ}\text{C}$ to $250\text{ }^{\circ}\text{C}$. It can be used in aerospace, oil and gas exploration, automotive electronics, nuclear industry, and in other fields where the ability of electronic devices to withstand high-temperature environments is strongly required. By utilizing a SC (Switched Capacitor) notch filter, the op amp achieves low input offset in a power-efficient manner. The circuit features a multi-path nested Miller compensation structure, consisting of a low-speed channel and a high-speed channel, which switch according to the input signal frequency. The input-stage operational amplifier is a fully differential, rail-to-rail design, utilizing tail current control to reduce the impact of common-mode voltage on the transconductance of the input stage. The two-stage operational amplifier uses both cascode and Miller compensation, minimizing the influence of the feed-forward signal path and improving the amplifier's response speed. The prototype op amp is fabricated in a $0.15\text{ }\mu\text{m}$ SOI process and draws 0.3 mA from a 5 V supply. The circuit occupies a chip area of 0.76 mm^2 . The measured open-loop gain exceeds 140 dB , with a 3 dB bandwidth greater than 100 kHz . The amplifier demonstrates stable performance across a wide temperature range from $-40\text{ }^{\circ}\text{C}$ to $250\text{ }^{\circ}\text{C}$, and exhibits an excellent input offset of approximately $20\text{ }\mu\text{V}$ at room temperature and an offset voltage temperature coefficient of $0.7\text{ }\mu\text{V}/^{\circ}\text{C}$ in the full temperature range.

Keywords: SOI; operational amplifier; high-temperature sensor; chopper

Academic Editor: Alessandro Lo Schiavo

Received: 4 December 2024

Revised: 11 January 2025

Accepted: 13 January 2025

Published: 16 January 2025

Citation: Yang, Z.; Li, J.; Fu, J.; Song, J.; Cai, Q.; Qiao, S. A $250\text{ }^{\circ}\text{C}$

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Applications. *Appl. Sci.* **2025**, *15*, 849.

<https://doi.org/10.3390/app15020849>

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1. Introduction

In specialized application scenarios such as aerospace, jet engines, and mine exploration [1–6], integrated circuit components must endure extremely harsh environmental and climatic conditions, where temperature fluctuations can significantly impact circuit performance stability. These applications typically require precision operational amplifiers with low noise, low offset, and high bandwidth to amplify weak signals in noisy environments. Such amplifiers are often the first devices in the measurement front-end, determining the system's dynamic range, sensitivity, and anti-interference capability. Most precision amplifiers use chopper technology, optimizing power and area efficiency to achieve low noise and offset without generating noise aliasing [7–11].

Ordinary integrated circuits are generally designed for room-temperature environments. The threshold voltage, carrier mobility, and PN junction leakage current of most semiconductor devices are significantly affected by temperature changes, making it difficult for chips to operate stably under large temperature variations. In high-temperature environments, the gain and noise performance often deteriorate dramatically, and there is even a risk of circuit failure [12,13]. Commercial CMOS technology platforms are typically qualified within the temperature range of $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$, as significant leakage currents arise at higher temperatures. However, in automotive, aerospace, power management, and oil and gas extraction applications, temperatures can exceed $200\text{ }^{\circ}\text{C}$ [14], as shown in Figure 1.

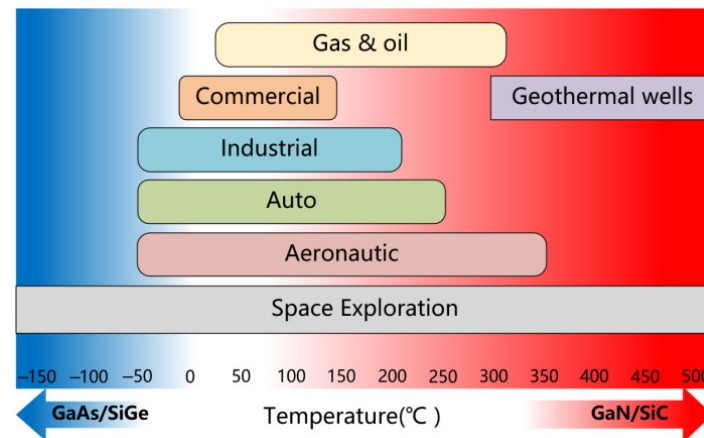


Figure 1. Temperature ranges for different electronics applications.

Researchers represented by Oucair published a series of papers in the 1980s on the changes in electrical characteristic indicators such as the threshold voltage, leakage source current, and carrier mobility of MOS field-effect transistors in the ambient temperature range of $25\text{ }^{\circ}\text{C}$ to $300\text{ }^{\circ}\text{C}$ [15,16], and proposed the classic Zero-Temperature Coefficient (ZTC) bias voltage theory [17,18], providing a theoretical basis for integrated circuit design in high-temperature ranges. Since the turn of the century, on the one hand, the theory and practice of integrated circuit design in the high-temperature range have been further developed, and on the other hand, the application and development of SiC materials have provided a good solution for the design of high-temperature integrated circuits, because SiC devices have excellent thermal stability and extremely low leakage current in high-temperature environments [19–22]. Research has shown that amplification circuits designed based on SiC technology can still exhibit good performance even in extremely high-temperature environments of $400\text{ }^{\circ}\text{C}$, which is incomparable to classical semiconductor materials such as Si, GaAs, SiGe, etc. [23–25]. However, the development level of SiC technology is still in its early stages, with immature technology, high cost, and low yield rate restricting its widespread application. Therefore, scholars are still mainly exploring and researching the design of high-temperature integrated circuits using relatively mature semiconductor processes.

SOI CMOS technology has demonstrated enhanced temperature capability, as its reduced substrate thickness enables low leakage current. SOI technology offers an effective solution for ensuring the high-temperature operation (up to $250\text{ }^{\circ}\text{C}$) of instrumentation amplifiers. Extensive research has been conducted on the performance and temperature compensation techniques of SOI CMOS devices, as well as other challenges associated with circuit operation at elevated temperatures [26–30]. Furthermore, a variety of

fundamental circuit modules have been successfully implemented using SOI CMOS technology [31–35].

In recent years, design strategies for low-noise amplifiers (LNAs) operating over high-temperature ranges have been broadly categorized into two approaches. The first involves employing the classic ZTC voltage bias technique, where the gate voltage of the MOS transistor is biased at the ZTC point to mitigate the temperature dependence of the LNA's performance. While this method can reduce temperature-related variations to some extent, not all transistors within the same process exhibit a well-defined and convergent ZTC point. Moreover, in many cases, locating such a point is challenging, limiting the effectiveness of this approach. The second approach dynamically compensates for temperature-induced changes in transistor characteristics by generating bias currents or voltages proportional to temperature. This method offers greater adaptability but is sensitive to manufacturing variations, which can compromise the accuracy of the compensation and, consequently, the performance of the amplifier. Both of these mainstream solutions provide the partial stabilization of gain and noise performance during temperature variations, but they remain constrained by inherent limitations. Therefore, further research is required to develop improved and optimized techniques that enable LNAs to function reliably over broader temperature ranges while maintaining stable performance metrics across varying thermal conditions.

The remainder of this article is organized as follows. Section 2 reviews the issues related to the design of low-offset operational amplifiers in high-temperature environments. Section 3 provides a detailed description of the implemented circuit. Section 4 presents the measurement results of the proposed operational amplifier. Finally, Section 5 concludes the paper.

2. Low-Offset Operational Amplifier

Common techniques for improving accuracy include tuning, automatic zeroing, and chopper techniques. Among these, tuning techniques can only suppress the initial offset and do not address the dynamic suppression of offset. In contrast, chopping and auto-zeroing are the two most widely used dynamic misalignment suppression techniques [36–39], and they will be discussed in detail in the following sections.

2.1. Chopping

Chopping stabilization technology is a modulation technique used to mitigate the impact of defects in operational amplifiers, including noise and offset voltage. With advancements in integrated circuit technology, choppers can be efficiently implemented on chips. Chopping operates by modulating the input signal, noise, and offset voltage to different frequencies, followed by low-pass filtering to produce a signal with reduced nonlinearity.

The simplified structure of the chopper amplifier is shown in Figure 2. The typical chopper amplifier consists of a chopper, amplifier, and demodulator. Among them, the input signal is modulated by the first chopper to the odd harmonic frequency of the chopping frequency. The amplifier amplifies the offset voltage, noise, and input signal, and then modulates it back to the initial frequency by the second chopper. The offset voltage V_{os} and noise V_n of the operational amplifier are only modulated to the chopping frequency by the output chopper and filtered by subsequent filters, thereby achieving the separation of the input signal V_{in} from the offset voltage and noise.

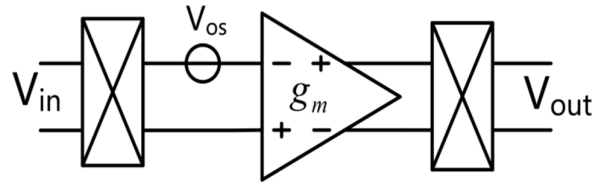


Figure 2. The structure of the chopper amplifier.

However, this method may introduce significant ripple. Several techniques are commonly employed to mitigate this ripple. One approach is to add a low-pass filter at the amplifier’s output; however, this reduces the available signal bandwidth. A second method involves using a multi-path amplifier topology, known as chopper stabilization, although this technique increases low-frequency noise. The third method incorporates a notch filter into the amplifier. A switched-capacitor notch filter can be synchronized with the chopper clock to filter out the ripple. This type of notch filter creates notches in the amplifier’s transfer function at the chopping frequency and its odd harmonics, which can be effectively mitigated through a multi-path topology.

The notch filter depicted in Figure 3 suppresses ripple by incorporating a switched-capacitor notch filter (SC-NF) after the output chopper. This amplifier builds upon the classic chopper amplifier design by adding a notch filter and two amplifiers, thereby enhancing its ability to resist interference, particularly in suppressing noise and common-mode disturbances. Unlike low-pass filters, the SC-NF selectively filters out ripples near the chopping frequency, leaving low-frequency signals unaffected. As a result, this method does not impact the overall bandwidth of the operational amplifier. The use of a notch filter is particularly efficient, as the switched-capacitor network does not consume any bias current.

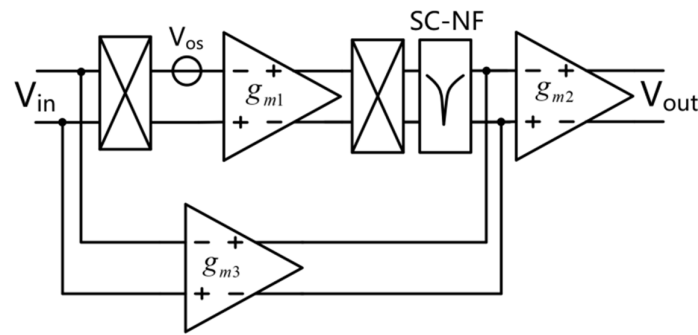


Figure 3. Chopper amplifier with SC notch filter.

2.2. Auto-Zeroing

Auto-zeroing technology is a sample and hold technique that can dynamically suppress the offset voltage, noise, and temperature drift in circuits. Automatic zeroing technology stores the sampled DC offset and noise in the sampling capacitor through sampling, and then subtracts it from the signal carrying DC offset and noise, ultimately achieving the goal of suppressing DC offset and noise. The basic principle of automatic zeroing is shown in Figure 4, which is controlled by a digital clock to sample switches S_1 - S_6 , and capacitors C_1 and C_2 are built around an operational amplifier g_m .

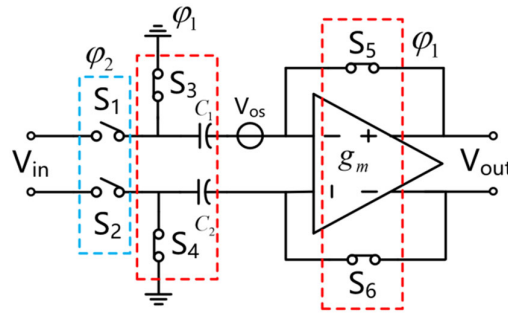


Figure 4. Auto-zeroing diagram.

Clocks ϕ_1 and ϕ_2 are complementary clocks, and the method of eliminating misalignment is usually carried out in two stages. The first stage is detection and storage. When the first clock phase ϕ_1 is at a high level, switches S_1 and S_2 are open, switches S_3 – S_6 are closed, and g_m is connected in a unity gain configuration. The offset voltage of the amplifier is stored in capacitor C_1 , as shown in (1).

$$V_A(f) = \frac{A}{1+A} V_{os} \tag{1}$$

The second stage is the amplification stage, in which the next clock phase ϕ_2 is at a high level. The amplifier g_m amplifies the input signal, which is then amplified by capacitors C_1 and C_2 before being further amplified by the amplifier. As shown in (2), the offset voltage V_{os} cancels out the voltage stored in capacitor C_1 . At this time, the input offset voltage of the amplifier is shown in (3), and the output only changes with the input differential voltage, not affected by the input offset voltage, thereby eliminating the offset voltage. Similarly, low-frequency flicker noise components are also stored on capacitors C_1 and C_2 , and therefore will be canceled out. However, the correlation between higher-frequency flicker noise components is small, so it cannot be effectively canceled out.

$$(V_{in} + \frac{A}{1+A} V_{os} - V_{os}) A = -V_{out} \tag{2}$$

$$V_{OS_in} = -\frac{A}{1+A} V_{os} \tag{3}$$

Additionally, according to the sampling theorem, the sampling process can induce high-frequency thermal noise outside the desired bandwidth to mix with in-band noise. This interaction increases the noise power spectral density (PSD) within the band, resulting in a higher in-band PSD compared to the original noise floor. The noise suppression effect of automatic zeroing technology is illustrated in Figure 5. As shown, under automatic zeroing conditions, low-frequency noise is primarily flicker noise, while in the absence of automatic zeroing, low-frequency noise is predominantly white noise. However, noise aliasing leads to an increase in the spectral density of baseband noise.

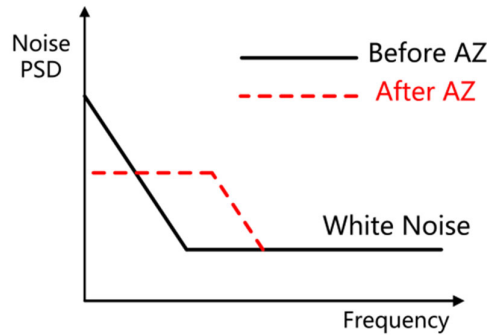


Figure 5. Noise spectrum before and after auto-zeroing.

Automatic zeroing technology offers a larger bandwidth and smaller ripple in the output voltage but comes with increased current consumption and a higher susceptibility to signal superposition, which results in elevated low-frequency noise. In contrast, chopping technology is less prone to signal superposition, but it has a narrower bandwidth, higher energy consumption, and significant output ripple at the chopping frequency. However, chopping technology generally requires lower power consumption. A comparison between the two technologies is presented in Table 1.

Table 1. Comparison between chopping and auto-zeroing.

Auto-Zeroing	Chopper Stabilized
Very low offset	Very low offset
Sample-and-hold	Modulation/demodulation
Higher low-frequency noise due to aliasing	Similar noise to flat band (no aliasing)
Higher power consumption	Lower power consumption
Wide bandwidth	Narrow bandwidth
Lowest ripple	Higher ripple
Little energy at auto-zero frequency	Lots of energy at chopping frequency

3. Proposed Circuit Implementation

In the standard CMOS process, devices are isolated by reverse-biased PN junctions. As the temperature increases, the current through the reverse-biased PN junction grows exponentially, leading to a significant increase in leakage current. In contrast, in the SOI process, devices are isolated by silicon dioxide insulating dielectrics, which substantially reduce leakage current and help prevent latch-up. Therefore, the circuit in this chapter is designed using the SOI process.

Although SOI process devices exhibit smaller leakage currents and a better suppression of latch-up, the electron mobility and threshold voltage of MOS devices still vary with temperature. This results in a reduction in parameters such as drain current and transconductance as temperature increases. To ensure circuit stability, the same input-stage structure and bias current are maintained across each amplifier stage. This approach ensures that, when the temperature changes, the input-stage transconductance of each stage undergoes nearly identical variations, thereby preserving overall frequency stability.

Additionally, the input stage operates in constant current mode. In the weak inversion region, where the current is low, the change in transconductance is primarily influenced by leakage current, leading to significant temperature-induced variation. In the strong inversion region, the change in transconductance is mainly driven by electron mobility, but the variation is considerably smaller than in the weak inversion region. To counteract the drop in input stage transconductance at high temperatures, a Proportional-To-

Absolute-Temperature (PTAT) current source is employed, which mitigates the temperature effects and helps maintain overall frequency stability.

3.1. MNMC and Frequency Compensation Method

The circuit adopts a multipath nested Miller compensation op-amp circuit structure, which consists of a low-speed channel composed of g_{m1} , g_{m2} and g_{m3} op amp, a chopper modulation circuit, and a notch filter in the blue area, as well as an NMC (nested Miller compensation) op amp and a high-speed channel SMC (single Miller compensation) op amp composed of g_{m3} and g_{m4} . When the input signal is at a low frequency, the overall gain is mainly provided by the low-speed channel. At high frequencies, the gain is mainly provided by the high-speed channel. The overall circuit structure is shown in Figure 6.

The low-speed channel is actually a three-stage op amp using NMC compensation, which can be regarded as two nested two-level Miller compensation structures. The difference from the conventional NMC circuit is that the Miller capacitor of the outer loop here is divided into two parts before and after the notch filter. This design choice is based on the fact that the output signal of the post-stage notch filter lags behind the input signal by one clock cycle. By feeding back the output to the notch filter both before and after, the output waveform becomes more continuous.

The high-speed channel g_{m4} will produce a left-half-plane zero LHP [40]:

$$z_1 = \frac{g_{m1} \cdot g_{m1}}{(C_{m2} + C_{m3})g_{m4}} \tag{4}$$

In order to maximize the bandwidth of the op amp, it can be used to offset the second pole of the low-speed channel NMC ($z_1 = p_2$). Finally, the third pole p_3 is designed at a high frequency outside the bandwidth to increase the phase margin [40].

$$p_2 = \frac{g_{m3}}{2C_L} \left(1 - \sqrt{1 - \frac{4g_{m2}/C_{m2}}{g_{m3}/C_L}} \right) \tag{5}$$

The main pole and the secondary main pole are located at very low frequencies, and the third pole p_3 is outside the bandwidth. The final system function is similar to a two-pole system. The Bode plot will form a frequency response with a 20 dB/dec roll-off starting from the low-frequency part.

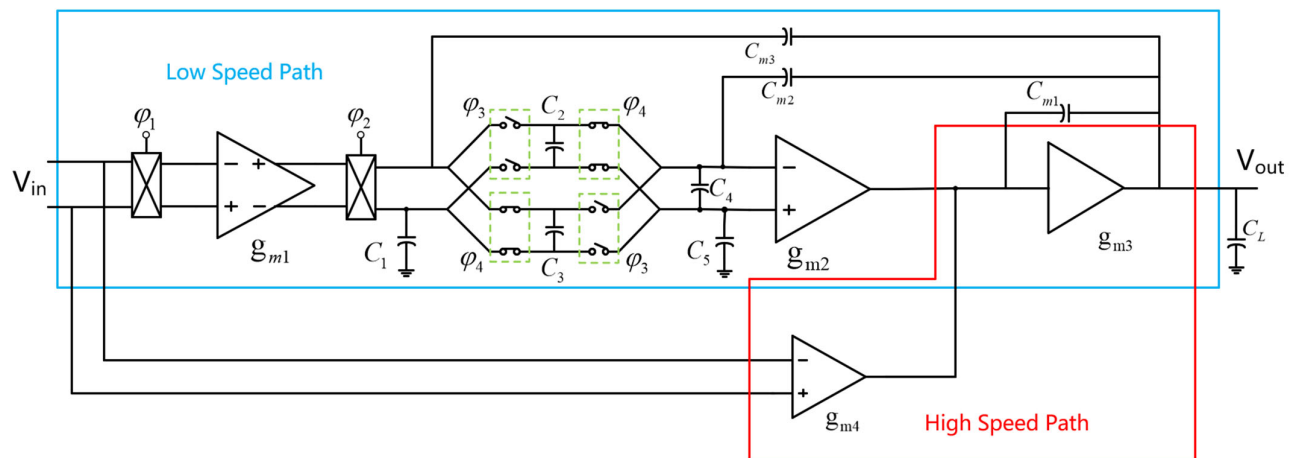


Figure 6. Overall circuit structure composition.

3.2. Design of Input-Stage Operational Amplifier

The input-stage op amp is a fully differential input rail-to-rail op amp. The design of the input-stage operational amplifier is shown in Figure 7. As the input-stage common-mode voltage changes from positive to negative, the input pair experiences three states: only PMOS is off, NMOS and PMOS work at the same time, and only NMOS is off. In this process, the input-stage transconductance change curve is a bell-shaped curve, the maximum value is twice the minimum value, and the frequency response curve is also the same. This requires good frequency compensation, and it is necessary to pay attention to the transient distortion caused by the fast-changing common-mode voltage modulating the input-stage transconductance.

To overcome the above problems, the input-stage differential pair circuit of the op amp adopts tail current control technology. By using current-switch MP15, as well as current-mirror MN2 and MN3 to provide bias for the input NMOS differential pair, the total current of the NMOS and PMOS differential pairs is a constant value. In this way, when the common-mode voltage is high and the PMOS differential pair is off, the current generated by the current source MP1 can still make the NMOS work. When the common-mode voltage is less than the reference level, the input-stage differential pair is dominated by PMOS. When the common-mode voltage is equal to the reference level, the NMOS and PMOS differential pairs work simultaneously. At this time, the input-stage transconductance is the largest, which is $\sqrt{2}$ times that of NMOS or PMOS working alone, reducing the influence of the common-mode voltage on the input-stage transconductance [41].

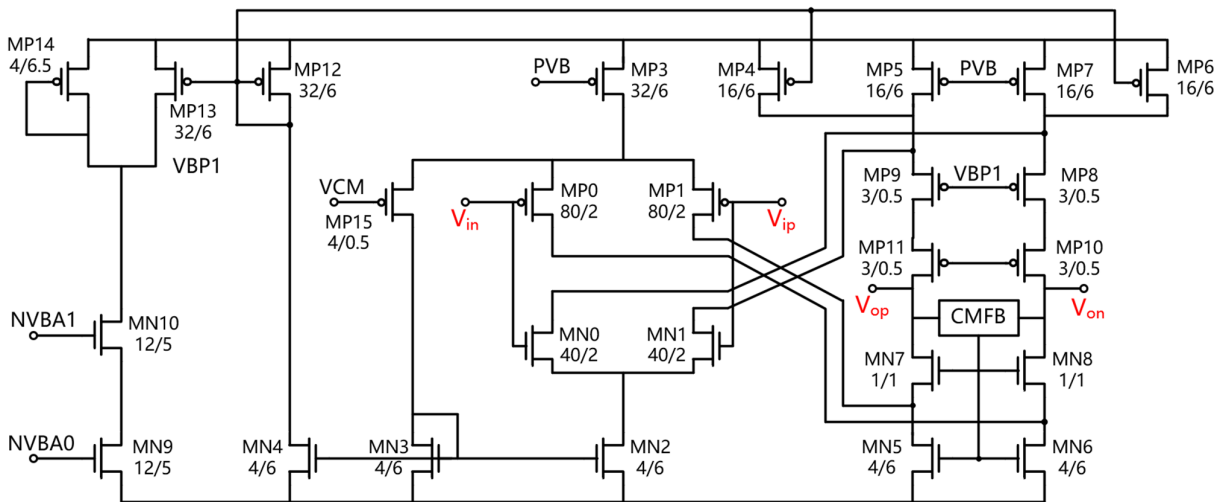


Figure 7. Input-stage operational amplifier circuit.

The NMOS differential input pair features two common-gate stages, while the PMOS differential input pair has only one common-gate stage. This design choice is primarily aimed at increasing the output impedance. To prevent significant variation in the overall gain with changes in the input common-mode voltage, a common-gate gate voltage adjustment circuit is also incorporated. This circuit ensures that the VBP1 voltage increases as the input common-mode voltage rises, thereby adjusting the intrinsic gain of transistors MP8 and MP9.

3.3. Notch Filter

In order to reduce the output noise, on the one hand, the chopper-stabilized circuit will transfer the output noise PSD from low frequency to high frequency. The chopping frequency of the op amp should be higher than the noise corner frequency. On the other

hand, it is necessary to add an LPF in the post-stage of the chopper-stabilized op amp to weaken the noise at high frequency and the higher harmonics caused by chopping.

As shown in Figure 8, the circuit consists of two sampling circuits and an adder [42]. During the ϕ_1 period, the capacitor C_{1B} samples the input signal V_{in} and transfers the charge from C_{1A} to C_2 ; during the ϕ_2 period, the capacitor C_{1A} samples the input signal V_{in} and transfers the charge from C_{1B} to C_2 . The charge after such a cycle is the sum of the two transferred charges. The overall circuit is actually equivalent to a sample-and-hold circuit, so the frequency response of the notch filter is a SINC function, and the gain is close to 0 when the input frequency is an even multiple of the chopping frequency. The spectrum of the notch filter is shown in Figure 9. In order to filter the periodic spike signals caused by the front-end chopper switch, the notch filter's stop frequency needs to be the same as the chopper frequency, and the clock of the switch in the notch filter needs to be delayed by $T/4$ cycles compared to the clock of the chopper switch to avoid the influence of spike pulses.

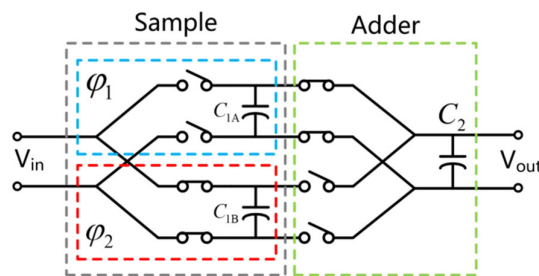


Figure 8. The notch filter circuit.

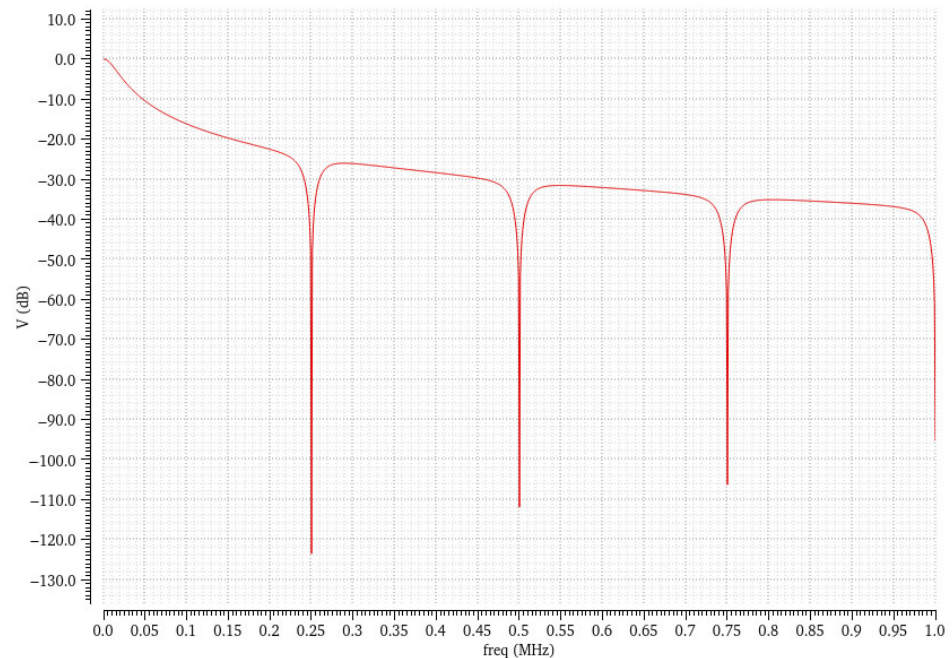


Figure 9. The spectrum of the notch filter.

3.4. Post-Stage Amplifier

In the overall circuit, g_{m2} and g_{m4} form a current summing circuit, so in the actual circuit, the two are designed in the same op amp. As shown in Figure 10, the circuit consists of an input rail-to-rail differential pair g_{m4} , an NMOS differential pair g_{m2} , a Class-AB

output stage circuit g_{m3} , Miller compensation capacitors, common source, common-gate stage compensation, and a Class-AB drive circuit.

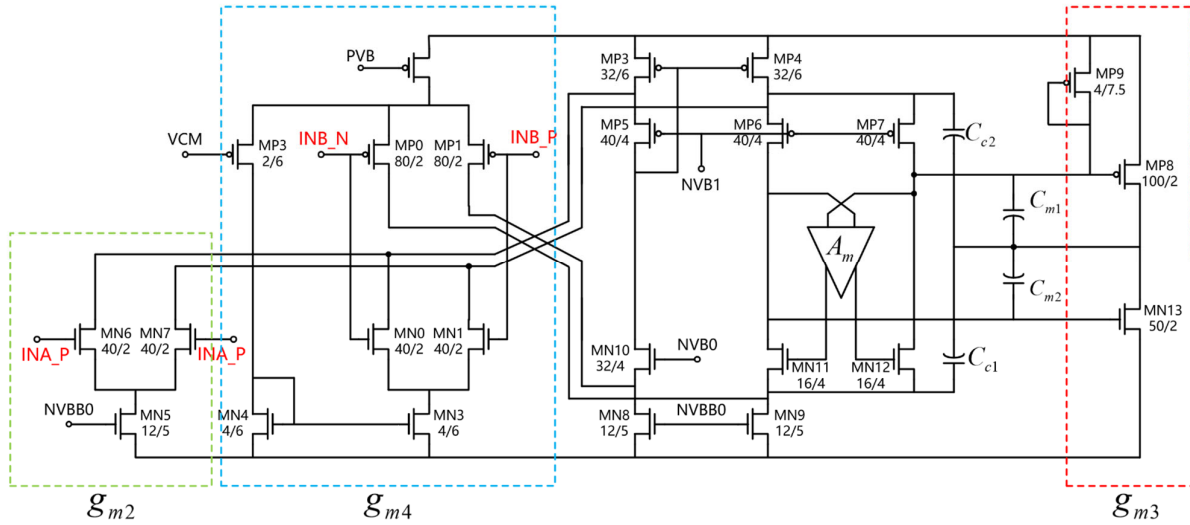


Figure 10. Post-stage operational amplifier circuit.

3.5. Class-AB Output and Drive Circuit

In order to maintain a balance between low static power consumption and high gain when the Class-AB output circuit is working, a fixed voltage difference is required between the NMOS and PMOS gates. In a static state, a smaller voltage can be maintained between V_{gsn} and V_{gsp} , which not only reduces static power consumption but also helps to increase output impedance and thus increase gain. In a dynamic state, the small signals of V_{gsn} and V_{gsp} are completely inverted, and g_{mn} and g_{mp} have opposite trends.

The gain of Class-AB is

$$G_{AB} = (g_{mn} \hat{v}_{gsn} - g_{mp} \hat{v}_{gsp}) \cdot R_{out} = (g_{mn} + g_{mp}) \cdot R_{out} \hat{v}_{in} \quad (6)$$

where

$$g_{mn} = K_n \frac{W}{L} (V_{GSn} - V_{THn}) \quad (7)$$

$$g_{mp} = K_p \frac{W}{L} (VDD - V_{AB} - V_{GSn} - V_{THp}) \quad (8)$$

In order to maintain a fixed voltage difference between the NMOS and PMOS gates, a differential difference amplifier (DDA) and MN11 and MN12 are designed in the circuit to form a Class-AB drive circuit [43].

Compared with the fully differential op amp, the differential op amp adds a pair of differential pairs, which can realize such operations.

$$V_{OP} - V_{ON} = A[(V_{PP} - V_{PN}) - (V_{NP} - V_{NN})] \quad (9)$$

The differential operational amplifier is connected to transistors MN11 and MN12 to form a regulated cascode structure. The difference between the drain voltages of MN11 and MN12, detected by the DDA, is compared to a reference voltage and output to the gate of the transistors, forming a negative feedback loop that stabilizes the drain DC

voltage. This negative feedback also reduces the gain of the common-gate stage involving MN11 and MN12, which in turn reduces the overall gain of the op amp.

In the circuit, g_{m2} and g_{m3} constitute a two-stage op amp. Miller compensation will produce a right-half-plane zero due to the existence of a feedforward signal path, reducing the phase margin and response speed of the op amp [44]. Cascode compensation does not have a feedforward path, and the response speed is greatly increased, but cascode compensation will produce a complex plane pole. When the capacitance is large, a gain spike may be generated at the pole position, reducing the gain margin of the op amp. This design uses cascode compensation and Miller compensation at the same time, which weakens the influence of the feedforward signal path of Miller compensation and increases the response speed of the op amp.

4. Measurement Results

The prototype op amp is fabricated in a 0.15- μm SOI Bipolar-CMOS-DMOS (BCD) technology and its micrograph is shown in Figure 11. The total chip area is approximately $800\ \mu\text{m} \times 950\ \mu\text{m}$. It consumes 0.3 mA current from a 5 V supply.

The operational amplifier designed in this paper works at $-40\ ^\circ\text{C}$ to $250\ ^\circ\text{C}$. Conventional bulk silicon CMOS devices face serious leakage and threshold voltage V_{th} drift problems at high temperatures, especially above $125\ ^\circ\text{C}$. The SOI process can solve the leakage problem due to its natural structural characteristics. Combined with the interconnection process and special doping treatment, it can effectively solve the problem of threshold voltage V_{th} drift with temperature.

The measurement setup used to characterize the performance of the op amp is shown in Figure 12. The system was tested across a wide temperature range from $-40\ ^\circ\text{C}$ to $250\ ^\circ\text{C}$ to evaluate its robustness and stability under extreme operating conditions. The results from this extensive temperature range are crucial for assessing the performance and reliability of the amplifier in high-temperature environments, as detailed in the following sections.

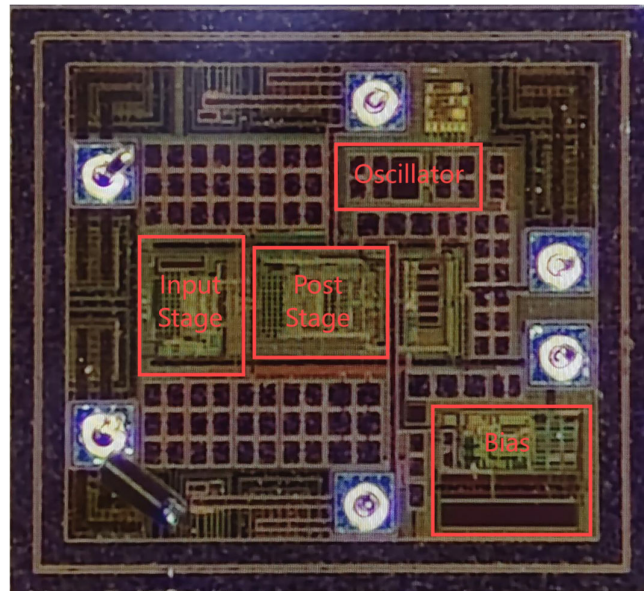


Figure 11. The chip micrograph.

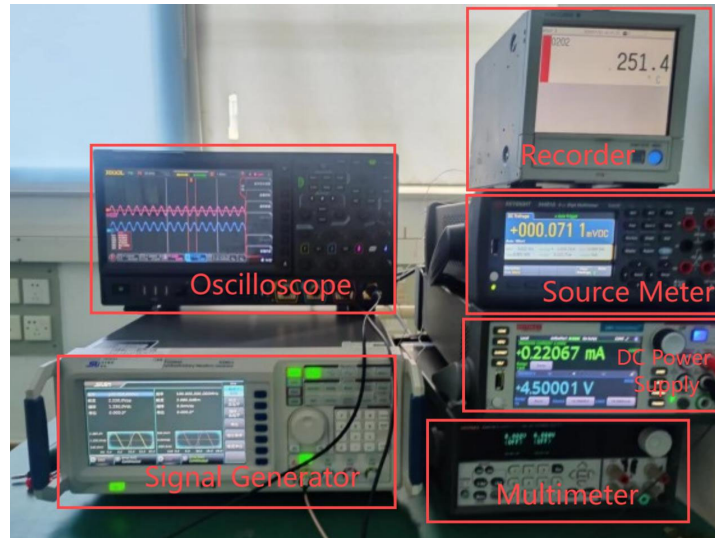


Figure 12. Measurement setup.

The frequency response of the operational amplifier was first evaluated with a 100 pF load capacitor at 250 °C, and the resulting open-loop gain is depicted in Figure 13. The blue curve represents the overall frequency response of the operational amplifier, while the red curve represents the frequency response of the high-speed channel. As shown, the low-frequency gain is primarily determined by the low-speed channel, while at higher frequencies, the gain of the high-speed channel dominates, coinciding with the overall gain. At this point, the overall gain is predominantly governed by the high-speed channel. The maximum open-loop gain at low frequencies reaches 140 dB. However, due to the overall frequency response rolling off with a slope of 40 dB per decade, the gain–bandwidth product (GBW) is approximately 100 kHz. This performance highlights the effectiveness of the multi-path hybrid nested Miller compensation, which enables stable operation over a wide range of frequencies while maintaining a high gain at low frequencies.

In a subsequent test, the op amp was configured as a unity-gain buffer, and the small-signal frequency response was measured using a 5 V step input signal with a cycle time of 10 ms. The results of this test are shown in Figure 14. This configuration demonstrates the op amp’s ability to maintain linearity and stability in response to a rapid input signal transition, further validating its performance under varying operating conditions.

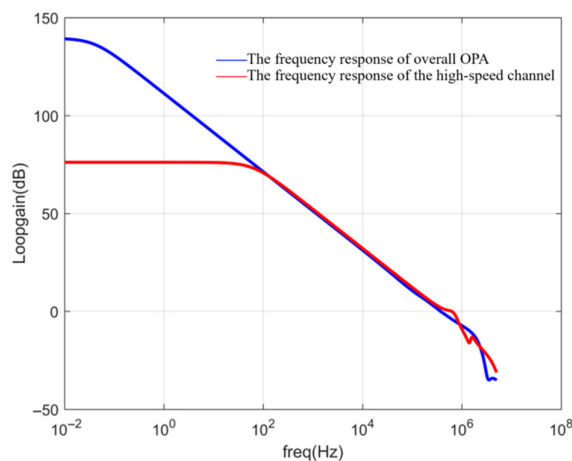


Figure 13. Open-loop gain (with a 100 pF load capacitor at 250 °C).

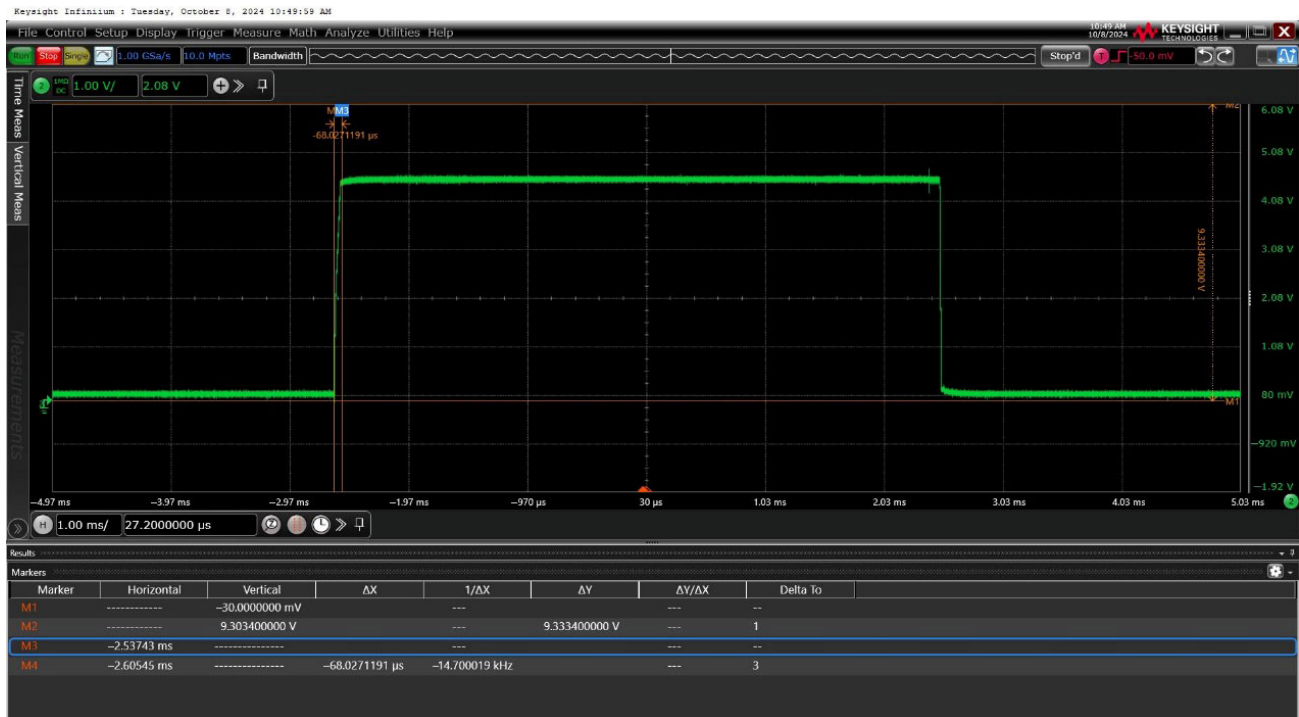


Figure 14. Pulse response (with a 5 V step input signal with a cycle time of 10 ms).

Table 2 summarizes the important parameter test results of the chip at room temperature. It can be seen that under a static current of 0.3 mA, both an offset voltage of 20 μV and a GBW of 0.1 MHz are ensured, as well as 140 dB. Furthermore, the operational amplifier demonstrates rail-to-rail input and output, ensuring a wide input range and maximizing the output voltage swing.

Table 2. Typical parameters of the amplifier at room temperature.

Parameter	TYP.	Unit
Quiescent current	0.3	mA
Input offset voltage	20	uV
Input offset voltage drift	0.7	uV/°C
Common-mode voltage range	2.5	V
Open-loop voltage gain	140	dB
Slew rate	0.45	V/μs
Gain–bandwidth product	100	KHz

To verify the amplifier’s operation in the targeted temperature range between −40 °C and 250 °C, extensive measurements have been performed. The temperature regulation involves placing the chip into a temperature chamber, and its model is MC-811B-2. The measurement results of some key parameters of the circuit vary with temperature, as shown in Figure 15. These parameter variations indicate the circuit’s stability under temperature changes, ensuring its proper operation in high-temperature environments.

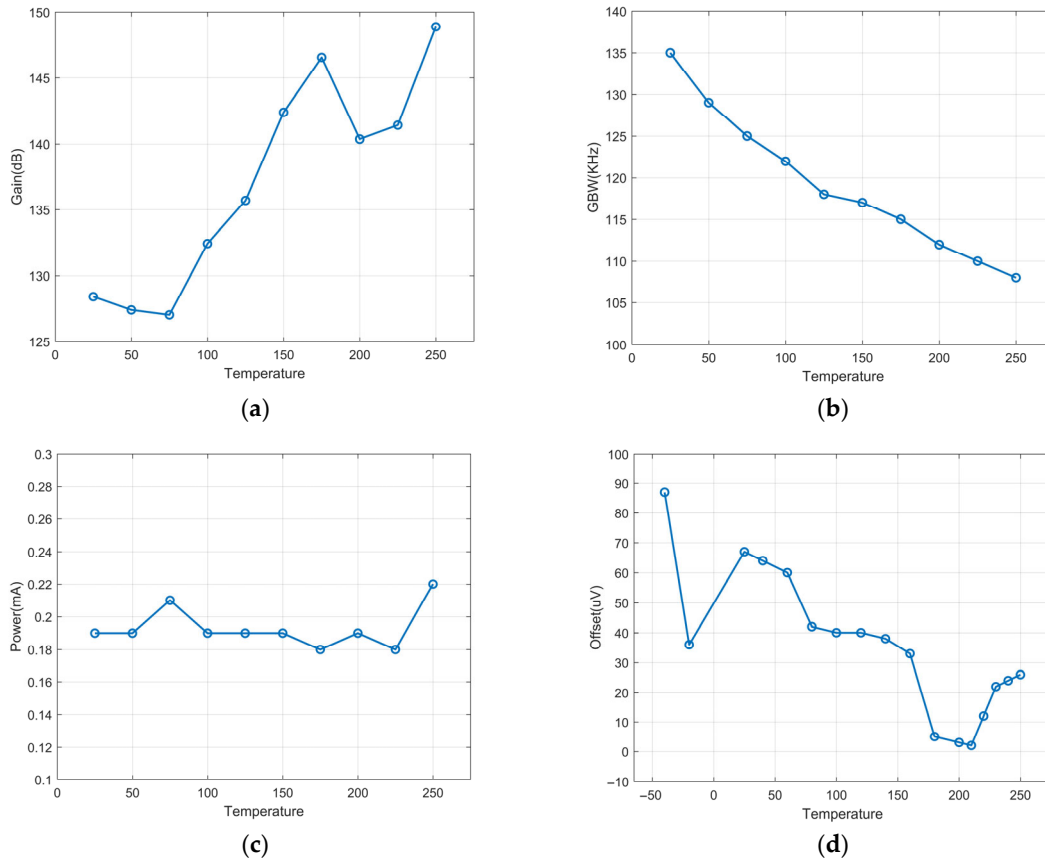


Figure 15. Measurement results versus temperature: (a) gain; (b) GBW; (c) power; (d) offset.

Table 3 summarizes and compares the performance of the operational amplifier in high-temperature applications. As shown, the amplifier achieves an offset voltage as low as 20 μV and a high DC gain of 140 dB, demonstrating its suitability for precision applications in demanding environments. These results underscore the amplifier’s ability to maintain exceptional performance, even under extreme temperature conditions, ensuring stability and reliability across a wide operational range.

Table 3. Comparison with previous work.

	This Work	[23]	[26]	[32]
Process	0.15 μm SOI BCD	4H-SiC	SOI-CMOS	-
Supply voltage (V)	5	7.5	3.3	3.0
Power (mW)	1	180	3.3	3.9
DC gain (dB)	140	34	25.7	108
BW (KHz)	100	100	500	9700
Input offset (μV)	20	-	10000	250
Active area (mm^2)	0.76	1.65	0.85	-
Temp. range ($^{\circ}\text{C}$)	-40–250	25–500	-40–170	-40–210

5. Conclusions

This paper presents a chopper-stabilized operational amplifier for high-temperature applications. The multipath nested Miller compensation structure, along with an SC notch filter, is proposed to reduce input offset and ripple. The amplifier has a high DC gain (140

dB) and bandwidth (100 KHz) with rail-to-rail input and output signal range. Compared with a traditionally structured op amp, this work achieves a lower offset while being more efficient in terms of power and area. The effectiveness of the proposed op amp has been demonstrated over a wide temperature range from $-40\text{ }^{\circ}\text{C}$ to $250\text{ }^{\circ}\text{C}$. Finally, this op amp also exhibits excellent power efficiency, input noise, and offset voltage. As a result, $20\text{ }\mu\text{V}$ offset and $0.7\text{ }\mu\text{V}/^{\circ}\text{C}$ maximum drift are achieved over the rail-to-rail input range. As a result of the above characteristics, this chip can be used in fields such as aerospace, oil and gas exploration, automotive electronics, and nuclear industry, where there is a strong demand for electronic devices to withstand high-temperature environments, such as amplifying and filtering pressure sensors, as well as temperature and humidity sensors in analog front-end application circuits.

Author Contributions: Conceptualization, Z.Y. and J.L.; methodology, J.F.; validation, J.S.; writing—original draft preparation, Z.Y.; writing—review and editing, Z.Y. and Q.C.; visualization, J.F.; supervision, S.Q.; project administration, S.Q. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the National Key Research and Development Program of China under Grant 2021YFB3202704.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data provided in this study are available upon request from the corresponding author. The data are not available to the public due to the confidentiality of the related R&D products.

Conflicts of Interest: The authors declare no conflicts of interest.

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