This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

Stability Analysis and Auto-Tuning of Interlinking Converters Connected to Weak Grids

Qing Liu, *Student Member, IEEE,* Tommaso Caldognetto, *Member, IEEE,* Simone Buso, *Member, IEEE*

***Abstract*—This paper presents an adaptive multi-loop control scheme for inverters interlinking dc voltage sources to single-phase, low voltage ac grids. Control self-adaptation is particularly useful in the case of weak grids that, due to frequent physical modifications (e.g., network reconfigurations, disconnection of generators/loads) and intrinsic lack of inertia, present strongly time-variant characteristics. The solution presented in this paper is based on a high-performance converter controller with auto-tuning capabilities. It is shown that the applied auto-tuning method can significantly widen the stability region of the interlinking converter, covering a broad range of grid impedance values. In addition, within the stable region, the controller maintains the nominal performance. Experimental results are reported validating the proposed approach in realistic operating conditions, including grid voltage distortion and variations of amplitude and frequency.**

***Index Terms*—auto-tuning; grid-connected inverter; interlinking converter; microgrids; stability.**

I. Introduction

RENEWABLE energy resources, such as photovoltaic (PV) and wind farms, are nowadays more and more integrated in electrical power systems, contributing to the limitation of fossil fuel consumption. The integration process involves the electrical infrastructure at all levels, from high-voltage three-phase to low-voltage single-phase grids. Small-scale PV sources and batteries, especially, are typically being integrated directly into the latter, often at the consumer's premises [1]–[5], and coordinated by local dispatchers or controllers [6], [7]. State-of-the-art buildings, indeed, integrate resources organized in smart hybrid nanogrids, which, thanks to suitable control and communication devices, ensure the highest flexibility and efficiency in hosting ac as well as dc loads and sources. Hybrid nanogrids represent the target application of the converter controller discussed in this paper, whose purpose is to provide an interface between the dc and the ac domains.

Typically, low-voltage single-phase grids are characterized by limited power capability and mainly resistive connection impedances, which, due to the varying power absorption from loads and the intermittent power generation from renewables, bring to grid parameters that are variable both from point to point and over time. The IEEE standard 1204 [8] describes the behavior of an ac power system by stiffness measures that refer to both static and dynamic performance indexes. The short-circuit ratio (SCR) is an index referring to the static grid behavior, being defined as the ratio between the short circuit power and the power of the installed generator. On the other hand, the dynamic grid characteristics are evaluated in terms of inertia, that is, by the capability of the ac power system to keep the grid frequency constant in the presence of variations in the power flow. Stiff grids, namely, grids whose voltage is negligibly affected by power flow and load characteristics, show high SCR and inertia; *vice-versa*, grids whose voltage is significantly affected by power flow variations are said to be weak and typically show both low SCR and low inertia. These non-ideal characteristics make the control of the inverters tied to weak grids particularly challenging.

In these conditions, the typical stability assessment methods, like those based on the Middlebrook criterion [9], are complicated by the uncertain and typically time varying characteristics of the grid impedance. Indeed, although a series resistive-inductive structure is always maintained [10], both the magnitude and the X/R ratio of the grid impedance are subject to significant variations among the different inverter connection sites and over time. Several papers have shown how suitably shaping the converter output impedance by control design effectively enhances the converter-grid connection stability. From this standpoint, control bandwidth maximization and control delay minimization [11], active damping techniques [12], [13], proper feed-forwarding strategies [14] are all effective provisions. Grid synchronization methods [15] may also be source of relevant stability issues. Grid synchronization is often performed by a phase-locked loop (PLL), whose performance affects the low-frequency behavior of the converter, especially under weak-grid conditions [16]. While this instability may be conveniently exploited in some situations [17], it is in general an issue that require dedicated provisions, like, for example, the tuning of the PLL regulator based on grid impedance estimations [18].

But, beside maintaining stability, a grid-tied converter should be capable of tolerating or, better, rejecting different kinds of exogenous perturbations often encountered in weak grids. These range from voltage frequency or amplitude variations to voltage harmonics that, if not dealt with properly, lead to more detrimental effects, like increased distribution losses, wearing of components (e.g., transformers windings), circulating harmonic currents. A satisfactory performance is therefore as important as stability.

Solutions documented in the literature that aim at complying with power quality standards [19] include repetitive controllers

Qing Liu and Simone Buso are with the Department of Information Engineering, University of Padova, Padova, 35131, Italy (e-mail: `name.surname`@dei.unipd.it). Tommaso Caldognetto (*corresponding author*) is with the Department of Management and Engineering and with the Interdepartmental Centre Giorgio Levi Cases, University of Padova, Vicenza, 36100, Italy (e-mail: tommaso.caldognetto@dei.unipd.it).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

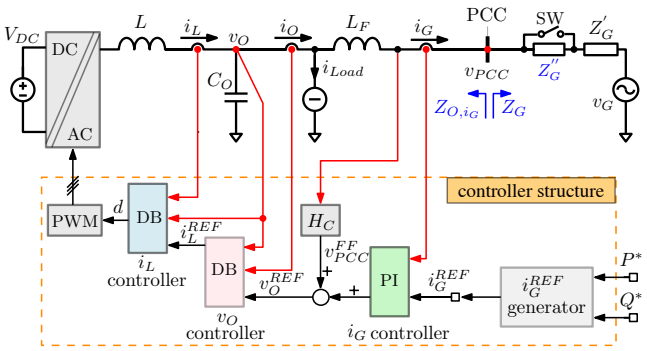


Fig. 1: Large-bandwidth triple-loop control system. Z_G is the total grid impedance, typically affected by uncertainty and varying over time.

[20], resonant controllers [21], [22], feed-forward of the PCC (point of common coupling) voltage [23], feedback of capacitor voltage [24]. Unfortunately, achieving robust stability and performance at the same time is difficult, because provisions that give stronger benefits in stability tend to penalize the inverter performance and the other way round.

The solution proposed in this paper aims at overcoming this undesirable trade-off. It is based on the triple-loop control structure shown in Fig. 1. The inductor current, capacitor voltage, and grid current are simultaneously controlled by high-performance implementations of predictive and digital proportional-integral (PI) controllers as shown, modeled, and experimentally validated in details in [25]. It has been shown [5] that this structure is potentially capable of outstanding performance and of mitigating many typical weak grid issues, such as circulating harmonic currents or grid voltage and frequency perturbations. In this paper, the robustness of this controller is analyzed considering, in particular, the effect of the grid characteristics at the point of connection. An *auto-tuning technique* is then developed that adapts the controller to the actual grid characteristics, yielding a much wider stability region and robust performance. The proposed auto-tuning technique *i*) requires minimal *a-priori* knowledge of the grid impedance at the point of connection, *ii*) shows little sensitivity to grid voltage harmonics and other perturbations (i.e., ensures robust performance), and *iii*) can be adapted and applied to any digital PI controller.

This paper extends [26], presenting additional analyses and experimental results. The reminder is organized as follows. Sec. II presents and summarizes the features of the considered triple-loop control structure. The stability of the controller is analyzed loop by loop in Sec. III, highlighting that only the third, grid-current control loop is affected by grid impedance uncertainty and requires the re-tuning of its parameters to keep optimal performance. The adopted auto-tuning technique is then analyzed in Sec. IV, where a design procedure is derived and the improvements on the grid/inverter connection stability are described. In Sec. V, the controller performance is evaluated experimentally while Sec. VI concludes the paper.

II. Review of the Large-Bandwidth Triple-Loop Inverter Controller

The considered large-bandwidth, triple-loop controller is shown schematically in Fig. 1. We now recapitulate its main characteristics.

A. Structure

The controller is made-up of inductor current i_L, output voltage v_O, and grid current i_G nested control loops. The inner loops are regulated by deadbeat-type controllers, aiming at maximizing the bandwidth of the outer grid current loop, which is governed by a discrete-time, proportional-integral (PI) controller. The following control equations are implemented.

1) Inductor current controller:

$$d(k) = \frac{\tilde{L} f_{sw}}{V_{DC}} \cdot \left[i_L^{REF}(k) - i_L(k) \right] + \frac{v_O(k)}{2V_{DC}} + \frac{1}{2}\,, \qquad (1)$$

where $\tilde{L}$ is the modeled value of the filter inductance L and the inductor current i_L is sampled *twice per switching period,* so that the duty-cycle update period is $T_{sw}/2$.

2) Output voltage controller:

$$i_L^{REF}(n) = \tilde{C}_O f_{sw} \cdot \left[v_O^{REF}(n) - v_O(n) \right] + i_O(n), \qquad (2)$$

where $\tilde{C}_O$ is the modeled value of the output capacitance C_O and v_O is sampled *once per switching period,* namely, the current reference update period is T_{sw}. To better highlight the difference with the previous equation, that is fundamental to explain the dynamic performance of the controller, index n is used in (2) instead of k.

About the delays and, in particular, computation times involved in performing (1) and (2), nowadays, implementations are available that achieve computation times amounting to a negligible fraction of the sampling period. For the considered application, as is detailed in Sect. V, the computation time is only 25 ns over the 25 µs sampling period. In case these issues were of some interest, as was often the case in the past, computation times can be taken into account as done, for example, in [27].

3) Grid current controller:

$$v_O^{REF}(n) = \mathrm{H}_{i_G}^{PI} \cdot \left[i_G^{REF}(n) - i_G(n) \right] + v_{PCC}^{FF}(n)\,, \qquad (3)$$

where $\mathrm{H}_{i_G}^{PI}(z) = K_p + K_i \cdot z/(z-1)$ is the grid-current regulator and the grid-current i_G is again sampled at every switching period T_{sw}. The grid current reference i_G^{REF} is calculated based on the active and reactive power to be delivered, namely P^* and Q^*, respectively, in Fig. 1, which may be issued, for example, by an external dispatcher, as discussed in Sect. I.

It is worth remarking that the multi-loop control scheme in Fig. 1 results in the implementation of a current source with current reference i_G^*. In principle, the current reference i_G^* can be set in any of the different ways applicable to converters operating as current sources. Commonly, i_G^* generation makes use of a PLL to derive references that are in-phase and in-quadrature with respect to the grid voltage, in order to ease the generation of active and reactive output power terms, associated to the in-phase and quadrature components,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

respectively [6], [15]. It is known that the use of PLLs to this purpose may bring to low-frequency (e.g., a few Hz) stability issues in particular operating conditions [16], even if the current control system is stable. These require dedicated analyses and provisions (see, e.g., [17], [28], [29]). Being the focus of this paper on the stability analyses and auto-tuning of the considered current control system, having crossover frequencies in the kHz range, specific PLL-related issues are not further discussed herein.

B. Features

As discussed in [25], the triple-loop controller shows valuable features for the implementation of interlinking converters, like *i*) excellent reference tracking, *ii*) uninterrupted high-quality local voltage supply, *iii*) strong attenuation of inverter-side and grid-side harmonics, *iv*) seamless transitions between grid-connected and islanded operation modes, *v*) resilience to grid perturbations.

C. Uncertainty effects

Uncertainty in converter and grid parameters, in general, negatively affects the stability of the grid-converter connection and the quality of the achievable performance. In the particular case of Fig. 1, the inner inductor current i_L and capacitor voltage v_O loops are controlled by a couple of dead-beat type controllers, (1) and (2), whose stability only depends on the accuracy of parameters $\tilde{L}$ and $\tilde{C}_O$. Both can be quite precisely known in the design phase and, most of all, practically do not vary during operation (neglecting aging and other long-term phenomena). On the contrary, the grid-current PI regulator appearing in (3) is directly affected by the uncertain grid impedance parameters. In order to determine the proportional and integral gains of the regulator that match the target specifications for the closed-loop bandwidth and the phase margin, also the grid impedance should be known. Unfortunately, in the typical case, it can be only roughly estimated and, most of all, it can change significantly from site to site and over time. Therefore, while the inner loops can be expected to exhibit intrinsic robustness, the grid current loop stability and performance can certainly benefit from automatically adapting the regulator gains to the specific grid impedance conditions encountered.

III. Stability analysis

This section discusses the sensitivity of each control loop stability to the uncertainty affecting the regulator parameters. All equations assume steady-state operation and consider electrical variables averaged over the sampling period.

A. Stability of the inductor current control loop (i_L loop)

The inductor current loop is the innermost loop (see Fig. 1), regulated by the dead-beat controller (1). Considering symmetrical PWM and averaging the voltage applied to the inductor in any half of a modulation period, the following average-current equation can be written:

$$\overline{i_L}(k+1) = \overline{i_L}(k) + [2d(k)-1]\cdot\frac{V_{DC}}{2Lf_{sw}} - \frac{\overline{v_O}(k)}{2Lf_{sw}}, \quad (4)$$

where L is the actual filter inductance. From (1) and (4), the closed-loop transfer function between the inductor current and its reference is found to be given by:

$$W_{i_L}(z) = \frac{i_L(z)}{i_L^{REF}(z)} = \frac{\frac{\tilde{L}}{L}}{z-1+\frac{\tilde{L}}{L}}. \quad (5)$$

To maintain stability, the pole of this discrete-time transfer function must lie within the unity circle. Simple calculations show that if $|(\tilde{L}-L)/L| < 1$, namely, if the relative error of the modeled inductance value is less than $\pm 100\%$, the stability of the inductor current loop is guaranteed. It is worth remarking that, in deriving (4), the parasitic resistance of the inductor is neglected, under the assumption that its L/R time constant is in any case *orders of magnitude longer* than the averaging period. This assumption will be later verified by measuring the inductor ESR values in the considered test case.

B. Stability of the output voltage control loop (v_O loop)

Considering now two consecutive sampling periods of duration $T_{sw}/2$, it is possible to write the discrete-time dynamic equation for the average output voltage, that is given by:

$$\begin{aligned}\overline{v_O(k+2)} \;= \overline{v_O(k)} + \frac{1}{2C_O f_{sw}}\left[\overline{i_L}(k+1)+\overline{i_L}(k)\right] + \\ - \frac{1}{2C_O f_{sw}}\cdot\left[i_O(k+1)+i_O(k)\right],\end{aligned} \quad (6)$$

where C_O is the actual filter capacitance. Because the voltage controller updates i_L^{REF} every period T_{sw}, while the current controller operates with time step equal to $T_{sw}/2$, the current reference samples in (1) are actually constrained by the following relation:

$$i_L^{REF}(k+1) = i_L^{REF}(k) = i_L^{REF}(n). \quad (7)$$

Now, by $\mathcal{Z}$-transforming (6) and using (2) and (7), after some algebraic manipulations [25], the reference to output voltage transfer function can be derived as:

$$W_{v_O}(z) = \frac{\frac{\tilde{L}\tilde{C}_O}{LC_O}}{2z^2 - 2z(2-\frac{\tilde{L}}{L}) + \frac{\tilde{L}\tilde{C}_O}{LC_O} + 2(1-\frac{\tilde{L}}{L})}. \quad (8)$$

Provided that the inductor L is precisely modeled by the inner inductor current loop, namely, $\tilde{L}/L = 1$, (8) can be further simplified as:

$$W_{v_O}(z) = \frac{\frac{\tilde{C}_O}{C_O}}{2z^2 - 2z + \frac{\tilde{C}_O}{C_O}}, \quad (9)$$

where the uncertainty in the controller parameter C_O is explicitly represented. By sweeping the relative error of the capacitor [i.e., $(\tilde{C}_O - C_O)/C_O$], the poles of the transfer function (9) can be determined as shown in Fig. 2. Notably, an error lower than 100% for $(\tilde{C}_O - C_O)/C_O$ guarantees stability, being the maximum magnitude of the poles always smaller than unity. Of course, if the inner and/or the outer loop are not properly tuned, the controller dynamic performance might significantly differ from the nominal one. Nevertheless, both loops can be considered intrinsically robust, as the critical parameter

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

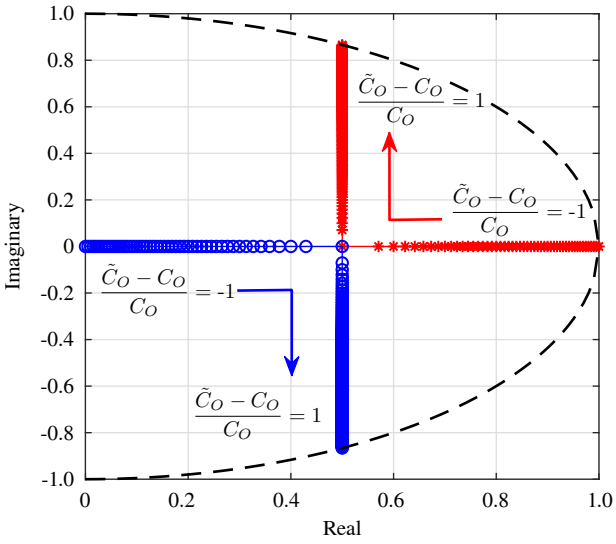


Fig. 2: Root locus of (9) with respect to variations of output capacitance C_O.

estimation error is much larger than the typical component tolerance.

C. Stability of the grid current control loop (i_G loop)

The stability of the grid-current loop can be analyzed considering its open-loop gain, that is:

$$T_{i_G}(z) = H_{i_G}^{PI}(z) W_{v_O}(z) \frac{1}{Z_{o,v_O}(z) + \tilde{Z}_G(z) + Z_{L_F}(z)}, \quad (10)$$

where, $\tilde{Z}_G$ and Z_{L_F} are, respectively, the estimated grid impedance and the grid-side inductor impedance while Z_{o,v_O} is the converter output impedance seen from the inverter output (i.e., filter capacitor C_O section in Fig. 1) when the inner loops are closed:

$$Z_{O,v_O}(z) = -\frac{v_O(z)}{i_O(z)} = \frac{1}{C_O f_{sw}} \frac{z-1}{2z^2 - 2z + 1}. \quad (11)$$

In the absence of any *a-priori* knowledge, $H_{i_G}^{PI}$ can only be designed based on reasonable assumptions on $\tilde{Z}_G$, like its resistive-inductive structure. A possibility is to consider it to be negligible (i.e., like in a strong, ideal grid), to design a stable control loop with desired bandwidth (e.g., 1.0 kHz) and phase margin (e.g., 45°) and then to verify the stability margins by considering the impedance ratio $Z_G/Z_{O,i_G}$, where Z_G is the actual grid impedance, measured at the PCC, while Z_{O,i_G} is the converter output impedance. The latter is given by:

$$Z_{O,i_G}(z) = -\frac{v_{PCC}(z)}{i_G(z)} = \\ = \frac{H_{PI}(z) W_{v_O}(z) + Z_{O,v_O}(z) + Z_{L_F}(z)}{1 - W_{v_O}(z) H_C(z)}, \quad (12)$$

where H_C is a feed-forward term that may be used to enhance the performance of the PI regulator (as shown in Fig. 1).

In general, any difference between $\tilde{Z}_G$ and Z_G affects the controller's bandwidth and phase margin, making them differ from the design values. To quantify the impact of the uncertainty, we may define the controller performance

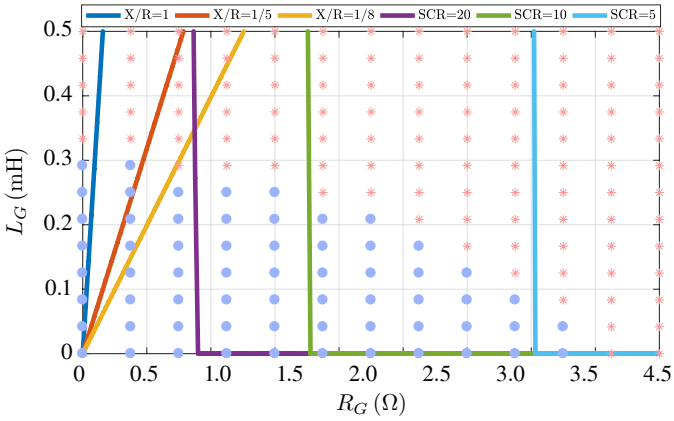


Fig. 3: Region of acceptable performance (blue dots) of the grid current loop; red crosses indicate points of low performance. Acceptable performance points have bandwidth ≥ 1 kHz and phase margin $\geq 45°$.

acceptable only when its closed loop bandwidth is larger than 1 kHz (i.e., 20 times the grid current frequency) and the phase margin is higher than 45°. It is then possible to derive the map of Fig. 3 that shows, in blue, the combinations of resistive (i.e., R_G) and inductive (i.e., L_G) components of Z_G that satisfy the acceptable performance criterion and, in red, combinations causing lower performance.

Noticeably, the performance of the grid current loop is not only related to the SCR (i.e., the magnitude of the grid impedance) but also to the X/R ratio [30]. For example, in the considered case of a 3 kVA single-phase interlinking converter, acceptable grid current control performance are achieved, for instance, when SCR > 20 and $X/R < 1/8$. In addition, the performance of the grid current loop degrades more with inductive grids (i.e., $X/R > 1$) than with resistive ones. In general, without any provision, grid current control performance degrades remarkably in weak grids. An auto-tuning technique that extends the stability region of the considered controller is presented in the following section.

IV. Auto-tuning method

The proposed method can be explained referring to Fig. 4. It exploits the estimation method discussed in [31] to automatically adjust the coefficients of the PI regulator $H_{i_G}^{PI}$ in the control system in Fig. 1. This allows to maintain the desired bandwidth and phase margin for the grid current control loop, guaranteeing optimized performance over a wider range of operating conditions. Please note that, in the following, a continuous-time modeling approach is adopted, although the implementation of the auto-tuner will be, in the end, fully digital. That is only possible because the sampling and algorithm iteration frequencies (i.e., 20 kHz in the case considered in Sect. V) are orders of magnitude higher than the tuner bandwidth (i.e., 100 Hz for the fastest loop considered in Sect. V). This allows to neglect the effects of discretization and to design the tuner as if it were a continuous-time system.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

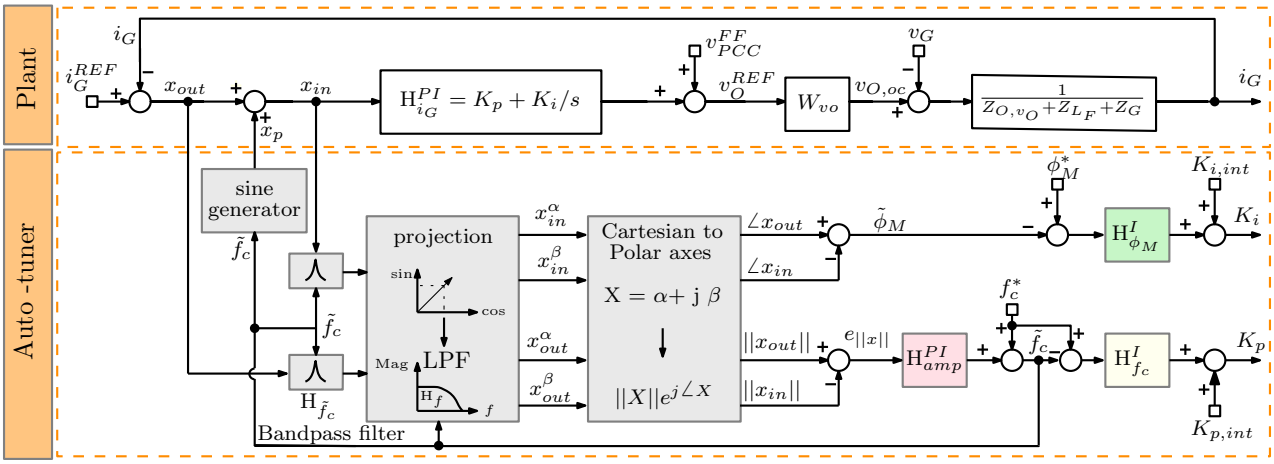


Fig. 4: Block diagram of the auto-tuning method, based on [31] and used to adjust the PI regulator $\mathrm{H}_{i_G}^{PI}$ in the control system in Fig. 1.

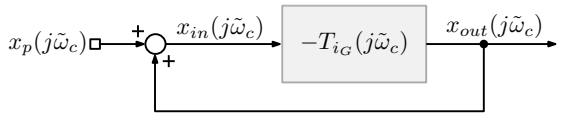


Fig. 5: Simplified block diagram of Fig. 4 considering the injecting frequency $\tilde{f}_c$.

A. Estimation of crossover frequency and phase margin

The auto-tuning technique is based on the injection of an adjustable-frequency, small-signal sinusoidal perturbation [i.e., $x_p(t) = |x_p|\sin(\tilde{\omega}_c t)$, $\tilde{\omega}_c{=}2\pi\tilde{f}_c$] that allows to monitor the crossover frequency, f_c, and the phase margin, ϕ_M, of the considered loop. With respect to the injected frequency and based on (10), the system block diagram in Fig. 4 can be simplified as shown in Fig. 5. In the steady-state, the relation between the measured signals x_{in} and x_{out} is:

$$\frac{x_{out}(j\tilde{\omega}_c)}{x_{in}(j\tilde{\omega}_c)} = -T_{i_G}(j\tilde{\omega}_c)\,. \tag{13}$$

As shown in Fig. 6, only at the true crossover frequency of the loop under test (i.e. when $\tilde{\omega}_c = \omega_c$), the magnitude of the loop gain satisfies:

$$|T_{i_G}(j\tilde{\omega}_c)| = \frac{|x_{out}(j\tilde{\omega}_c)|}{|x_{in}(j\tilde{\omega}_c)|} = 1\,. \tag{14}$$

Fig. 6 suggests that an accurate estimate of the grid current loop crossover frequency f_c can be obtained by adjusting the perturbation signal frequency $\tilde{f}_c$ so as to make the magnitude difference $|x_{out}| - |x_{in}|$ equal to zero. A PI compensator, H_{amp}^{PI}, can be used to this purpose:

$$\tilde{f}_c = f_c^* + \mathrm{H}_{amp}^{PI}\left(|x_{out}| - |x_{in}|\right)\,, \tag{15}$$

where f_c^* is the desired crossover frequency of grid current loop. Similarly, an estimate of ϕ_M is given by:

$$\begin{aligned}\tilde{\phi}_M &= \pi + \angle T_{i_G}(j\tilde{\omega}_c) = \\ &= \angle x_{out}(j\tilde{\omega}_c) - \angle x_{in}(j\tilde{\omega}_c)\,.\end{aligned} \tag{16}$$

Here, the amplitudes (i.e., $|x_{in}|$ and $|x_{out}|$) as well as the

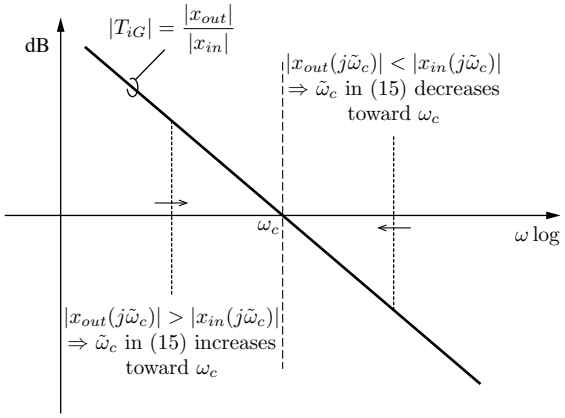


Fig. 6: Basic principle of crossover frequency identification based on T_{i_G}.

phases (i.e., $\angle x_{in}$ and $\angle x_{out}$) are estimated by performing projection onto a rotating frame synchronized with signal x_p and a cartesian to polar axes transformation. In order to extract just their components at $\tilde{f}_c$, x_{in} and x_{out} are pre-filtered by a band-pass filter $H_{\tilde{f}_c}$, implemented via a second-order generalized integrator (SOGI) with a peak frequency adaptively tuned to $\tilde{\omega}_c$ and suitably chosen selectivity gain k_f. Its transfer function is [32]:

$$H_{\tilde{f}_c}(s) = \frac{k_f\tilde{\omega}_c^2 s}{s^2 + k_f\tilde{\omega}_c s + \tilde{\omega}_c^2}\,. \tag{17}$$

An example of what can be observed considering x_{out} and x_{in} is presented in Fig. 11(c), which refers to the case when $|x_{out}| = |x_{in}|$ and, accordingly, $\tilde{f}_c = f_c$ and $\tilde{\phi}_M = \phi_M$.

B. Analysis of the auto-tuner

First of all, let us consider Fig. 7, which shows the open loop gain (10) with different choices of $\mathrm{H}_{i_G}^{PI}$. In the figure, T_{i_G} refers to a PI regulator with coefficients giving the desired f_c = 1 kHz and ϕ_M = 60 °, T'_{i_G} with the proportional coefficient doubled, and T''_{i_G} with the integral coefficient doubled. From

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

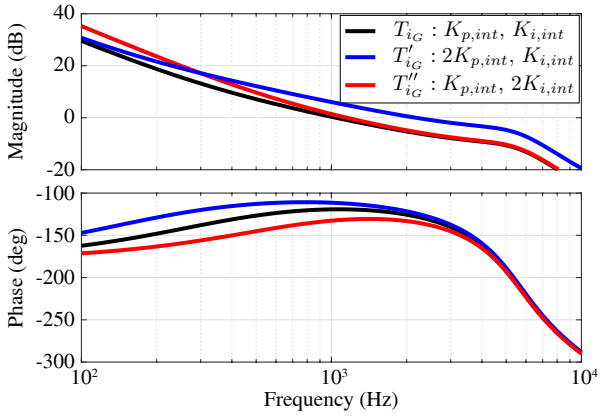


Fig. 7: Comparison of T_{iG} with different H_{iG}^{PI} coefficients.

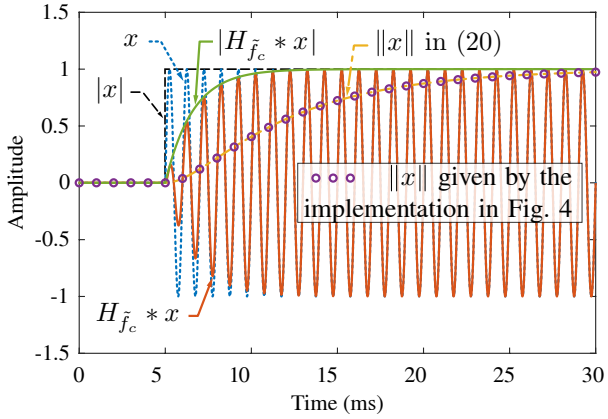


Fig. 8: Relations between the amplitude of x (i.e., $|x|$) with signal $H_{\tilde{f}_c} * x$ in (19) and signal $\|x\|$ in (20).

these plots, it is possible to notice that f_c is mainly linked to the proportional coefficient of H_{iG}^{PI}, while ϕ_M to the integral one. A more general approach can be based on the numerical calculation of the crossover frequency sensitivity to the controller gains. In the case here considered it is easily found that the crossover frequency presents a much higher sensitivity to the proportional gain than to the integral one. Accordingly, the principle of operation of the proposed tuning algorithm is to adjust K_p on the basis of the estimated f_c, and to adjust K_i on the basis of the estimated ϕ_M [33]. Therefore, as can be seen in Fig. 4, signals $\tilde{f}_c$ and $\tilde{\phi}_M$ are firstly compared with the respective reference values f_c^* and ϕ_M^*, then the error is closed-loop controlled to zero by the integral controllers $\mathrm{H}_{f_c}^{I}$ and $\mathrm{H}_{\phi_M}^{I}$. In particular, K_p is increased to increase $\tilde{f}_c$, while K_i is decreased to increase $\tilde{\phi}_M$.

C. Design of the auto-tuner

The design procedure for the regulators H_{amp}^{PI}, $\mathrm{H}_{\phi_M}^{I}$, and $\mathrm{H}_{f_c}^{I}$ in Fig. 4 is presented in the following.

1) Design of H_{amp}^{PI}*:* a dynamic model describing how the difference of the estimated amplitudes depends on the frequency of the injected perturbation signal is necessary for the design of H_{amp}^{PI}. To derive that model, namely, the transfer function $e_{\|x\|}(s)/\tilde{f}_c(s)$, recalling Fig. 4 and (13), x_{in} and x_{out} can be written in terms of x_p as:

$$\begin{cases} x_{in}(s) = \frac{1}{1+T_{iG}(s)} x_p(s) \\ x_{out}(s) = -\frac{T_{iG}(s)}{1+T_{iG}(s)} x_p(s) \end{cases} . \tag{18}$$

These signals are pre-filtered by the filter $\mathrm{H}_{\tilde{f}_c}$ in (17), whose response to a signal of the kind $x(t) = A_x \sin(\tilde{\omega}_c t)$ for $t \geq 0$ is the result of the convolution [32]:

$$\begin{aligned} \mathrm{H}_{\tilde{f}_c} * x(t) = & \frac{A_x}{\sqrt{1-\frac{k_f^2}{4}}} \sin\left(\tilde{\omega}_c \sqrt{1-\frac{k_f^2}{4}} t\right) e^{-\frac{k_f \tilde{\omega}_c t}{2}} + \\ & + A_x \sin(\tilde{\omega}_c t) \simeq A_x \left(1 - e^{-\frac{k_f \tilde{\omega}_c t}{2}}\right) \sin(\tilde{\omega}_c t) , \end{aligned} \tag{19}$$

where the last approximation holds on the assumption that $\tilde{\omega}_c \gg k_f \tilde{\omega}_c/2$, that is, the filter dynamics are very slow as compared to the period of the input signal, which is true in the considered application. Fig. 8 displays the relation among the amplitude of x and $\mathrm{H}_{\tilde{f}_c} * x$ in case $\tilde{\omega}_c = 2\pi\, 1\,\mathrm{krad/s}$ and $k_f = 1/5$. The transfer function between the amplitude $|x|$ and the estimated amplitude $\|x\|$ is given by the exponential term in (19), yielding

$$\frac{\|x\|(s)}{|x|(s)} = H_f(s) \cdot \frac{1}{1 + \frac{2}{k_f \tilde{\omega}_c} s}, \tag{20}$$

where H_f is the transfer function of the low-pass filter used to remove the second harmonic oscillations originating from synchronous demodulation in the projection block. It is worth highlighting that the filter $H_{\tilde{f}_c}$ allows to reject background components that may be present in the measured signals and extract just the signal component of interest, at $\omega_{\tilde{f}_c}$. The final relation among amplitude variations of x and the corresponding estimate $\|x\|$ is displayed in Fig. 8.

As can be seen, the amplitude estimation generated by (20) pretty much follows the envelope of the real implementation response. Furthermore, in both cases, the steady-state value is consistent with the amplitude of the input signal. The dynamic model of the amplitude response to frequency variations is therefore validated.

From (18) and (20), the amplitude error $e_{\|x\|}$ can be written as a function of $|x_p|$, that is:

$$\begin{aligned} e_{\|x\|}(s) &= [\|x_{out}\|(s) - \|x_{in}\|(s)] = \\ &= [|x_{out}|(s) - |x_{in}|(s)] \cdot \frac{H_f(s)}{1 + \frac{2}{k\tilde{\omega}_c} s} = \\ &= \frac{|T_{iG}(s)| - 1}{|T_{iG}(s) + 1|} \cdot \frac{H_f(s)}{1 + \frac{2}{k\tilde{\omega}_c} s} \cdot |x_p|(s) . \end{aligned} \tag{21}$$

In order to find the transfer function $e_{\|x\|}(s)/\tilde{f}_c(s)$ we observe that any small variation of $\tilde{f}_c$ turns into the variation of signals $|x_{in}|$ and $|x_{out}|$. The variations in the amplitudes of $|x_{in}|$ and $|x_{out}|$, will then turn into a variation of the amplitude error $e_{\|x\|}$, whose dynamic is determined by (20). If the auto-tuning process is designed to be significantly slower than the system to be tuned (e.g., by one or two orders of magnitude), these two phases of the dynamic process (21) can be decoupled and the estimator's one (20) can become dominant. This means

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

that the relation between a small-signal variation of $\tilde{f}_c$ and the variations of $|x_{in}|$ and $|x_{out}|$ can be considered instantaneous and its gain can be reasonably approximated by the partial derivative of the steady-state value of (21) at frequency $\tilde{f}_c$. The steady-state value of (21) is:

$$e_{\|x\|}\big|_{\text{dc}} = \frac{|T_{i_G}(j2\pi\tilde{f}_c)|-1}{|T_{i_G}(j2\pi\tilde{f}_c)+1|}\cdot|x_p|. \tag{22}$$

Its partial derivative, $\partial e_{\|x\|}\big|_{\text{dc}}/\partial\tilde{f}_c$, can be numerically calculated from (10) and (22). Under the above assumption, we can finally write the following approximated expression of the loop gain to be compensated:

$$\frac{e_{\|x\|}(s)}{\tilde{f}_c(s)} \approx \frac{\partial\, e_{\|x\|}\big|_{dc}}{\partial\tilde{f}_c}\cdot\frac{H_f(s)}{1+\frac{2}{k\tilde{\omega}_c}s}, \tag{23}$$

The regulator H^{PI}_{amp} can be designed now from (23), following any standard procedure. Herein, a bandwidth of 100 Hz (i.e., approximately a tenth of the system's crossover frequency) and a phase margin of 70° are adopted.

2) Design of $\text{H}^I_{\phi_M}$*:* to the purpose of designing the regulator $\text{H}^I_{\phi_M}$, a transfer function describing how the estimated phase margin changes with respect to the adjustments of the integral gain K_i is needed. Aiming at a tuning process that should be slow (e.g., with dynamics in the order of 0.1 to 1 s), the dynamics of the previously designed amplitude-difference control loop, having a crossover frequency of about a hundred Hz, can be neglected. Accordingly, the only relevant parameter in the design of $\text{H}^I_{\phi_M}$ is the dc gain $\partial\phi_M/\partial K_i|_{\text{dc}}$, which can be numerically evaluated by exploiting (10). A purely integral implementation of $\text{H}^I_{\phi_M}$, with a crossover frequency of 2 Hz, is here adopted.

3) Design of $\text{H}^I_{f_c}$*:* as done for the design of the previous regulator, the design of $\text{H}^I_{f_c}$ can be performed on the basis of the dc gain $\partial f_c/\partial K_p|_{\text{dc}}$, which can be numerically evaluated by exploiting (10). A purely integral implementation of $\text{H}^I_{f_c}$, with a crossover frequency of 0.5 Hz, is adopted for this regulator. Finally, it is worth remarking that mismatches in the estimated transfer function (10) can always occur. This aspect has to be taken into account in setting the design specifications of the regulators above (e.g., by setting adequate stability margins and requiring sufficiently slow response times to ensure the validity of the adopted models). So doing, a stable operation of the auto-tuning technique and optimal control performance can be achieved in cases of practical interest.

D. Effectiveness of the auto-tuner

The aim of the auto-tuner is to adapt the controller coefficients in order to keep the control bandwidth and phase margin of the grid current loop constant and, consequently, to get a robust controller performance when impedance characteristics change. The stability and performance of the controller, now equipped with the auto-tuner, are evaluated and reported in Fig. 9. As in Fig. 3, performance is considered acceptable when the bandwidth is $\geq$ 1kHz and the phase margin is $\geq 45°$. Again, the blue dot area indicates the region of acceptable performance; the red star area indicates lower bandwidth or phase margin. Compared with Fig. 3, with the auto-tuner, 1) the stability of the grid-inverter connection as well as an acceptable performance of the triple-loop controller are maintained in a much wider region of grid impedances, 2) the system can provide high performance not only with stiff grids (SCR $>$ 20), but also with weak grids (SCR $<$ 5). All these features are experimentally verified in the following section. Finally, it is also worth remarking that regions of not adequate performance (i.e., red dots in Fig. 9) will always exist: they correspond to unfeasible conditions in which, with the given controller and system structure, it is not possible to find any K_p and K_i parameter values that allow to obtain the desired crossover frequency and phase margin.

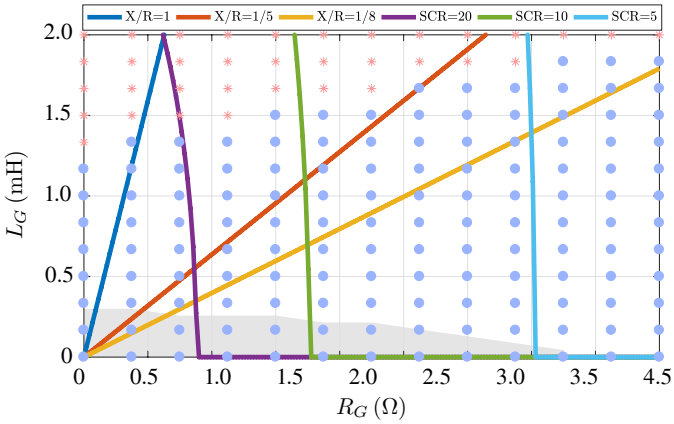


Fig. 9: Region of acceptable performance (blue dots) of the grid current loop (bandwidth $\geq$ 1 kHz, phase margin $\geq 45°$); red crosses indicate points of lower performance. For comparison, the shaded area is the acceptable performance region of Fig. 3.

TABLE I: System parameters

Parameter	**Symbol**	**Value**	
Nominal DC link voltage	V_{DC}	450	V
Switching frequency	f_{sw}	20	kHz
Filter inductance	L	1.40	mH
Inductor equivalent resistance	ESR_L	60	mΩ
Output capacitance	C_O	30	μF
Line inductance	L_F	0.55	mH
Inductor equivalent resistance	ESR_{L_F}	75	mΩ
Nominal power	S_O	3	kVA
Nominal voltage	V_N	230	V

V. Experimental Results

The proposed triple-loop controller equipped with the auto-tuning technique in Fig. 4 was applied to the interlinking-converter in Fig. 1. The main system parameters are listed in Tab. I. The control system is deployed on an NI cRIO-9068, based on a Xilinx Zynq 7020 all-programmable system on chip (AP-SoC) and equipped with suitable NI C Series modules for analog and digital input/output. The performed implementation in the FPGA of the adopted AP-SoC allows to complete the computation of (1)-(3) within 25 ns.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

In the following, the performance of the proposed control system is shown and discussed in terms of *i*) stability, considering parameters uncertainties, *ii*) auto-tuning effectiveness, *iii*) response to grid-impedance variations, *iv*) harmonic rejection capability. In the tests, the magnitude of the injected signal x_p (see Fig. 4) is 5% of the rated current. This value is a good trade-off between precision of detection and limitation of harmonic pollution. From experiments, a recommended magnitude range of x_p is found in the range [2%, 10%] of the rated current. In the practical case, to further limit the distortion of the grid current, x_p injection could be performed only intermittently.

A. Stability considering parameters uncertainties

The stability of the control loops is determined by the accuracy of system modeling, in particular, filter inductance $\tilde{L}$, capacitance $\tilde{C}_O$, and grid impedance $\tilde{Z}_G$ values (see Sect. III).

1) Inductor current loop: Fig. 10(a)-(c) show the small-signal step responses of the inductor current loop considering: *(a)* an underestimation of the filter inductance by 50% (i.e., $\tilde{L} = 0.5L$), *(b)* the exact value of the filter inductance (i.e., $\tilde{L} = L$), *(c)* an overestimation of the filter inductance by 50% (i.e., $\tilde{L} = 1.5L$). Fig. 10(a) and 10(c) highlight a detrimental effect on the inductor current regulation, which, however, keeps stable in both cases. Compared with Fig. 10(b), the inductor current in Fig. 10(a) shows slower dynamics (i.e., 4 steps) in tracking the current reference.

2) Output voltage loop: Similar tests are performed and reported in Fig. 10(d)-(f) for the output voltage loop, varying the value of the modeled output capacitance $\tilde{C}_O$, while not introducing errors in the inductance value (i.e., $\tilde{L} = L$). For a 50% underestimation of C_O [see Fig. 10(d)], a rise time T_r = 109 μs is measured, which is almost doubled compared with that of case Fig. 10(e), where T_r = 51 μs. In addition, it is also verified that a 50% overestimation of C_O [see Fig. 10(f)] does not cause unstable behaviors, neither in the inductor current nor in the output voltage. This shows the robustness of the controller with respect to mismatches in the inner loop parameter values.

3) Grid-current loop: The performance of the grid current loop is determined mainly by its bandwidth and phase margin. The PI controller of the grid current loop is designed based on (10) targeting 1 kHz bandwidth and 45° phase margin under ideal grid conditions (i.e., $\tilde{Z}_G$ = 0). Its sensitivity to time varying grid characteristics is now tested. A grid impedance variation is actuated by switch SW in Fig. 1: when SW is off, the grid impedance Z_G is the series of the impedance $Z_G^{'}$ (0.45 mH + 0.15 Ω) and an additional impedance $Z_G^{''}$ that can assume values $\{1\,\mathrm{mH}, 3.5\,\Omega, 1\,\mathrm{mH} + 3.5\,\Omega\}$, when SW is on, Z_G equals $Z_G^{'}$. A significantly distorted grid voltage is considered (THD_{v_G} is 4.86 %) and a non-linear load is connected in parallel with the output capacitor. The harmonic spectra of the grid voltage and the non-linear load current are reported in Tab. II.

Fig. 13(a) shows the controller's performance with the designed PI regulator ($K_{p,int}$ and $K_{i,int}$) under stiff and weak grid conditions in phases S1 and S2, respectively. In the stiff grid case S1 the total grid impedance is set to $0.45\,\mathrm{mH} + 0.15\,\Omega$ (SCR = 85.5). In the weak grid case S2 the total grid impedance is set to $1.45\,\mathrm{mH} + 3.65\,\Omega$ (SCR = 4.8). Due to the effect of the grid impedance, the measured crossover frequency and phase margin are far from the target values (i.e., $f_c^* = 1\,\mathrm{kHz}$ and $\phi_M^* = 45°$): 675 Hz and 64° in S1, 210 Hz and 56° in S2 are the measured values when the converter is connected to the considered grid.

TABLE II: Testing conditions of Fig. 13(j) under distorted grid voltage v_{PCC} and load current i_{Load}.

	% of rated voltage and current in Tab. I						
Order	**h1**	**h2**	**h3**	**h4**	**h5**	**h6**	**h7**
v_{PCC}	94.8	5.3	1.1	0.7	2.4	0.6	1.1
i_{Load}	18.9	0.7	14.7	0.3	8.3	0.1	2.9
Order	**h8**	**h9**	**h10**	**h11**	**h12**	**h13**	**h14**
v_{PCC}	0.1	0.5	0.1	0.1	0	0.1	0.1
i_{Load}	0.1	2.0	0.1	0.21	0.1	0.11	0.1
Order	**h15**	**h16**	**h17**	**h18**	**h19**	**h20**	
v_{PCC}	0.2	0	0.1	0	0.1	0	
i_{Load}	0.8	0.1	0.9	0.1	0.1	0	

B. Auto-tuning effectiveness

The auto-tuning is now introduced and shown in the basic case in which the converter is connected to a short circuit, with reference crossover frequency of 1 kHz and phase margin 60°. Initially, the controller of the i_G control loop is set with controller's parameters values computed off-line on the basis of the open loop gain T_{i_G}, the measured converter's parameters in Tab. I, and the output impedance $Z_G = 0$. Fig. 11(a) shows the signals x_{in} and x_{out} in steady-state when their amplitude are equal. By definition, it is therefore possible to measure the crossover frequency and the phase margin of the experimental setup for the considered loop, as discussed in Sect. IV-A; we found 702 Hz and 68°, respectively. In these conditions, Fig. 12(a) shows the obtained response to a step change of the current reference i_G^*, set as a piecewise constant value for this specific test. The resulting response is consistent with the measurements in Fig. 11(a), indeed, a slightly slower and more damped response than expected is obtained, which can be noticed by comparison with the superimposed dashed red line representing the response obtained by the simulation model. The differences in the dynamic responses are due to the unavoidable small mismatches between the modeled and the experimental systems.

Fig. 11(b) shows the behavior across the activation of the auto-tuning algorithm, which smoothly corrects the controller parameters values to match the given references of crossover frequency and phase margin. Notably, $K_p : 3.3 \rightarrow 4.3$ while $K_i : 0.14 \rightarrow 0.31$. Fig. 11(c) provides a zoomed-in view when the auto-tuning is activated and in steady-state. In this condition, it is possible to measure the final crossover frequency and phase margin after tuning, which

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

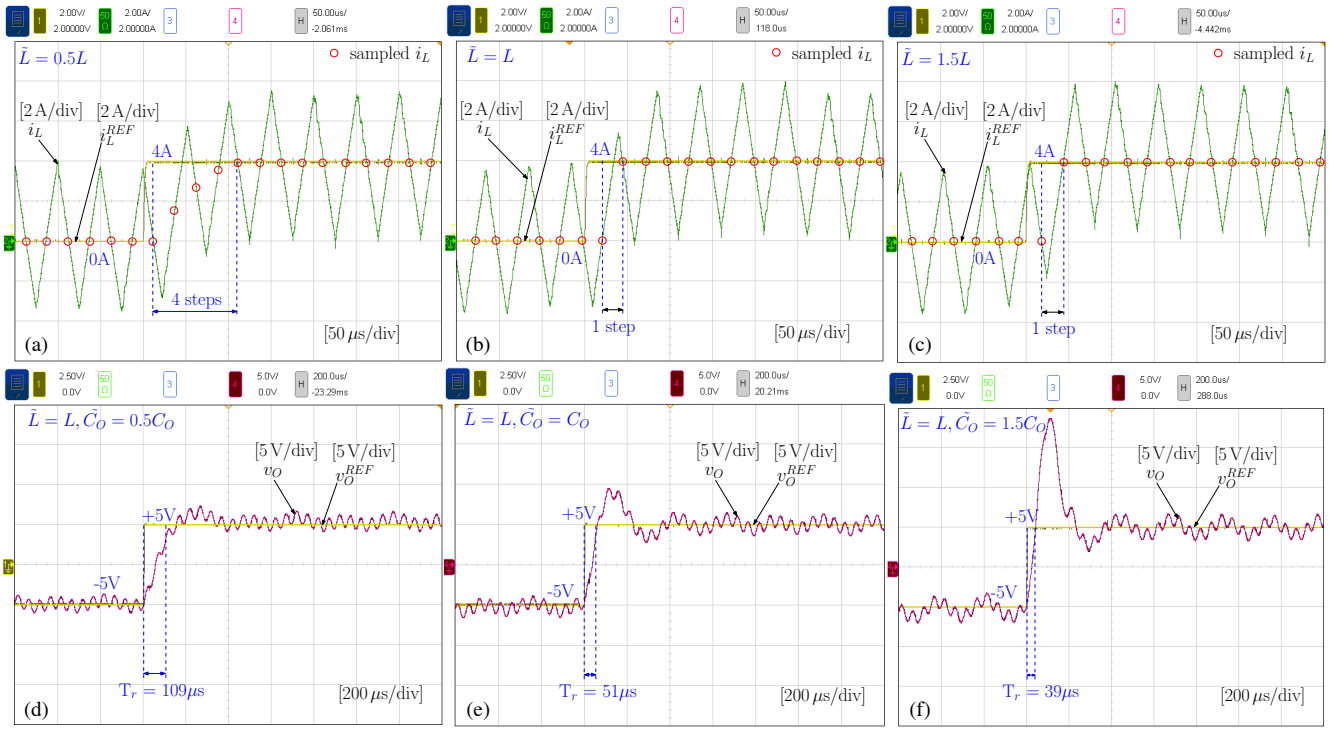


Fig. 10: Behavior of the inner loops if errors are introduced in the parameters of the control laws (1) and (2). Subfigures (a), (b), and (c) show the behavior of the i_L loop, subfigures (d), (e), and (f) show the behavior of the v_O loop.

actually correspond to the given references. Fig. 12(b) shows the step response obtained after tuning, it is possible to notice a close match between the simulation and experimental results, both in terms of obtained waveforms and measured rise-time and overshoot.

C. Response to grid impedance variations

The behavior of the proposed auto-tuning method while grid connected is now shown, considering different step variations of $Z_G = R_G + j\omega L_G$:

- *Auto-tuning activation Fig. 13(b):* with the system initially in the same conditions of S2 in Fig. 13(a), the auto-tuning is disabled during S1 and enabled during S2. Remarkably, the auto-tuner smoothly adjusts the parameters K_p and K_i to restore the target values of crossover frequency and phase margin.
- *From weak to stiff grid in Fig. 13(c):* a transition from a weak grid to a stiff grid condition is shown, where the total grid impedance changes from Z_G = 1.45 mH + 3.65 Ω, SCR = 4.8, in S1, to Z_G = 0.45 mH + 0.15 Ω, SCR = 85.5, in S2. The coefficients K_p and K_i are smoothly adjusted and $\tilde{f}_c$ and $\tilde{\phi}_M$ are automatically brought to the reference values, within 1 s from the applied change.
- *Step increase of R_G in Fig. 13(d):* a step increase in the grid resistance R_G is shown, where the total grid impedance changes from Z_G = 1.45 mH + 0.15 Ω in S1 to Z_G = 1.45 mH + 3.65 Ω in S2.
- *Step increase of L_G Fig. 13(e):* a step increase in the grid inductance L_G is shown, where the total grid impedance changes from Z_G = 0.45 mH + 3.65 Ω in S1 to Z_G = 1.45 mH + 3.65 Ω in S2.
- *From stiff to weak grid in Fig. 13(f):* a transition from a stiff grid to a weak grid condition is shown, where the total grid impedance changes from Z_G = 0.45 mH + 0.15 Ω, SCR = 85.5, in S1, to Z_G = 1.45 mH + 3.65 Ω, SCR = 4.8, in S2. A symmetrical behavior can be observed with respect to Fig. 13(c).

It is possible to remark that the proposed auto-tuner is capable of guaranteeing the desired bandwidth and phase margin in the considered testing conditions despite of significant variations in grid resistance and inductance.

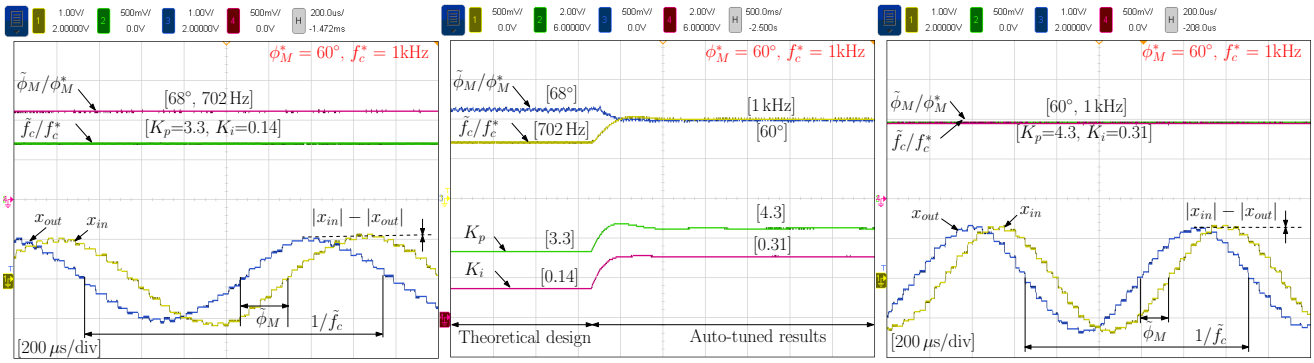
D. Harmonic rejection capability

Fig. 13(g)-(i) show the waveforms obtained during S1 of Fig. 13(a), S1 of Fig. 13(b), S2 of Fig. 13(b), respectively. The corresponding harmonic spectrum analysis of the grid current is reported in Fig. 13(j), grid and load harmonics are reported in Tab. II.

In the cases of Fig. 13(g) and Fig. 13(h), the auto-tuning is disabled and the measured bandwidth of the grid current loop is 675 Hz and 210 Hz, respectively, as reported in Sect. V-A3. The measured harmonic distortion is $\text{THD}_{i_G} = 2.55\%$ in Fig. 13(g) and $\text{THD}_{i_G} = 3.29\%$, in Fig. 13(h).

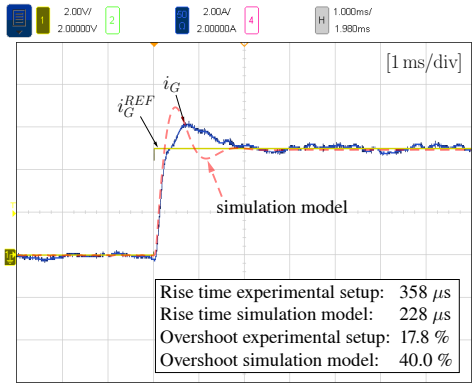
In the case of Fig. 13(i) the auto-tuner is active, keeping the grid current control loop crossover frequency always equal to the given reference of 1 kHz. Due to the higher crossover frequency and, consequently, loop gain of the current loop, with respect to the previous case in Fig. 13(h), the measured THD of the grid current reduces to 1.47%, as indicated in

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics

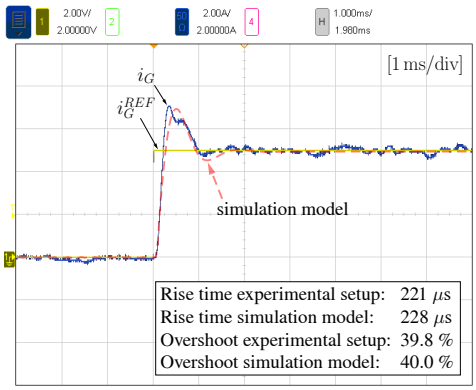


(a) Before applying auto-tuning (b) Auto-tuning activation (c) Auto-tuning enabled

Fig. 11: Auto-tuning process. (a) Monitored parameters of the i_G control loop before auto-tuning activation; controller's parameters set by design on the basis of T_{i_G} in (10) and the measured output impedance Z_G. (b) Dynamics of the auto-tuning when activated. (c) Monitored control loop parameters with auto-tuning active. (a) and (c) refer to the steady-state operation before and after, respectively, the auto-tuning activation shown in (b).



(a) Before applying auto-tuning



(b) After auto-tuning

Fig. 12: Step response of the grid current loop. (a) Before auto-tuning; controller's parameters set by design on the basis of T_{i_G} in (10) and the measured output impedance Z_G [conditions as in Fig. 11(a)]; (b) after auto-tuning [conditions as in Fig. 11(c)].

Fig. 13(h). This improvement is achieved without employing any further harmonic suppression provisions.

Finally, it is possible to notice that under the considered various testing conditions the harmonic content fulfills the IEEE Std. 1547 [19].

VI. Conclusions

An adaptive, high-performance control scheme is proposed for interlinking converters connected to weak, single-phase grids. The control scheme is developed based on a large-bandwidth triple-loop controller, on top of which an auto-tuning technique is implemented. Its purpose is to provide the on-line adjustment of the proportional and integral gains of the outer, grid current controller. The auto-tuner small-signal model is firstly derived, based on which design criteria are given for each of its inner regulators. The tuning strategy is then implemented in an FPGA control platform and experimentally tested. The experimental results prove that the auto-tuner can improve the grid connected converter performance in different ways. First of all, robust stability and performance are guaranteed in the presence of time-variant grid impedance characteristics, as often encountered in low-voltage single-phase ac microgrids. Second, a precise and fast control of the injected current is achieved and maintained, which allows the converter to be safely operated even in the presence of significant grid voltage distortion.

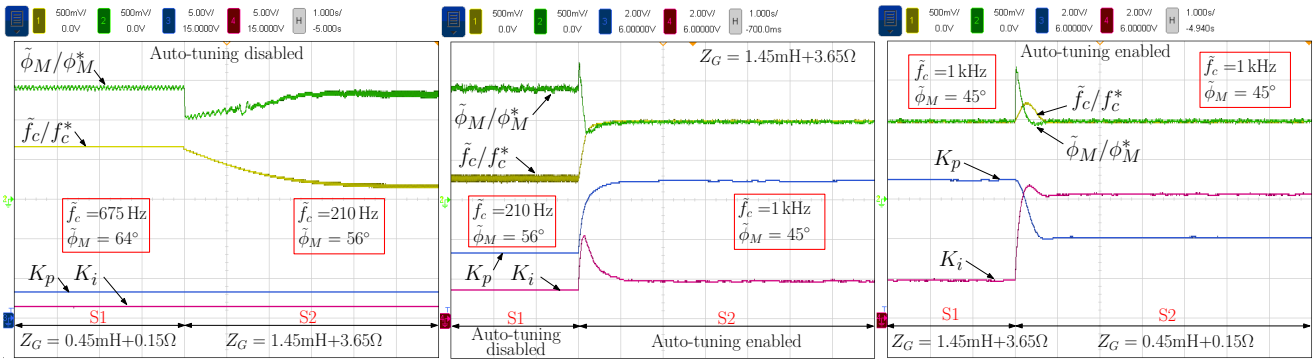
References

[1] Ó. Lucía, I. Cvetkovic, H. Sarnago, D. Boroyevich, P. Mattavelli, and F. C. Lee, "Design of Home Appliances for a DC-Based Nanogrid System: An Induction Range Study Case," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 4, pp. 315–326, Dec. 2013.

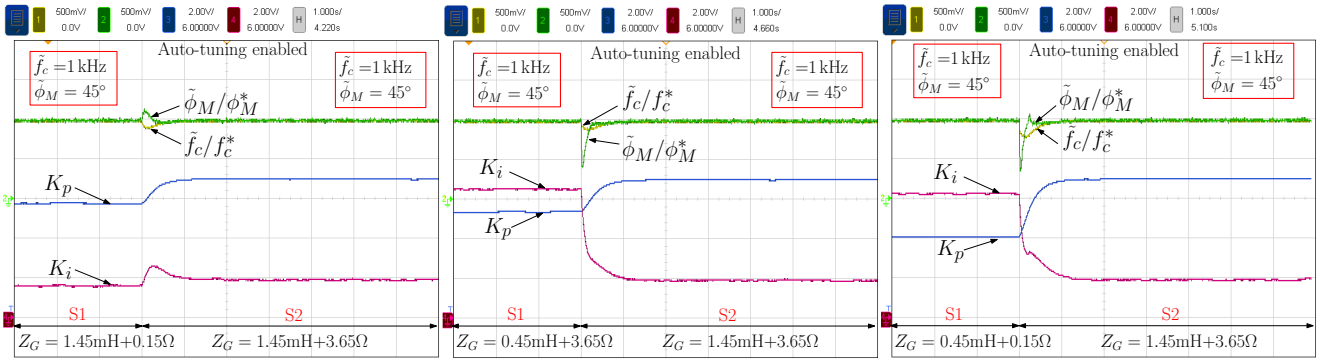
[2] M. Shahidehpour, Z. Li, W. Gong, S. Bahramirad, and M. Lopata, "A Hybrid ac/dc Nanogrid: The Keating Hall Installation at the Illinois Institute of Technology," *IEEE Electrification Magazine*, vol. 5, no. 2, pp. 36–46, Jun. 2017.

[3] A. Burgio, D. Menniti, N. Sorrentino, A. Pinnarelli, and M. Motta, "A compact nanogrid for home applications with a behaviour-tree-based central controller," *Applied Energy*, vol. 225, pp. 14 – 26, 2018.

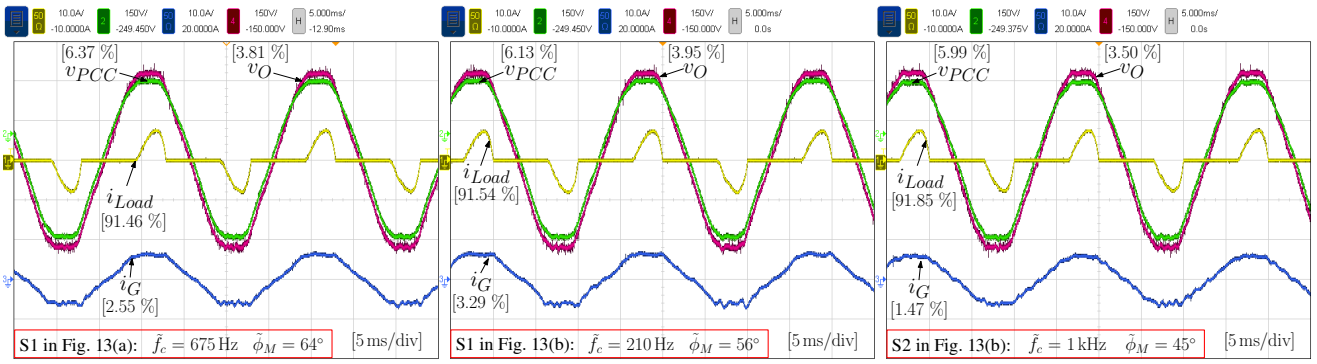
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2019.2899191, IEEE Transactions on Power Electronics



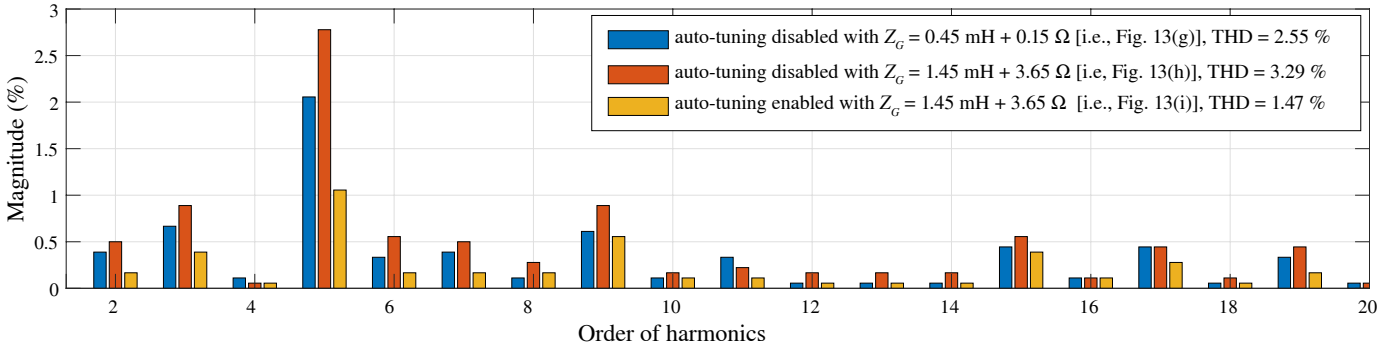
(a) Auto-tuning disabled with variation of Z_G (b) Auto-tuning from disabled to enabled (c) Variation from weak to stiff grid



(d) Step increase of R_G (e) Step increase of L_G (f) Variation from stiff to weak grid



(g) Waveforms during S1 of Fig. 13(a) (h) Waveforms during S1 of Fig. 13(b) (i) Waveforms during S2 of Fig. 13(b)



(j) Harmonic content of the grid current i_G in subfigures (g), (h), and (i)

Fig. 13: Performance of the triple-loop controller equipped with the proposed auto-tuning technique. **(a)** Response to grid impedance variations with auto-tuning disabled. **(b)** Auto-tuner from disabled to enabled–initial conditions set as in S2 of (a). **(c)** Grid impedance changed from resistive in S1 to inductive in S2. **(d)** Step change of grid resistance from $0.15\,\Omega$ to $3.65\,\Omega$. **(e)** Step change of grid inductance from $0.45\,\text{mH}$ to $1.45\,\text{m}\Omega$. **(f)** As in (c) but reversed. **(j)** Harmonic spectrum of the grid current in (g), (h) and (i); THD values are reported between brackets.

[4] M. Sechilariu, B. Wang, and F. Locment, "Building Integrated Photovoltaic System With Energy Storage and Smart Grid Communication," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1607–1618, Apr. 2013.
[5] Q. Liu, T. Caldognetto, and S. Buso, "Flexible Control of Interlinking Converters for DC Microgrids Coupled to Smart AC Power Systems," *IEEE Transactions on Power Electronics*, pp. 3477–3485, 2019.
[6] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, "Control of Power Converters in AC Microgrids," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734–4749, Nov. 2012.
[7] "IEEE Draft Standard for the Specification of Microgrid Controllers," *IEEE P2030.7/D11, August 2017*, pp. 1–42, Jan. 2017.
[8] *IEEE Std 1204-1997: IEEE Guide for Planning DC Links Terminating at AC Locations Having Low Short-Circuit Capacities*. IEEE, 1997.
[9] R. D. Middlebrook, "Input filter considerations in design and application of switching regulators," *IEEE Industry Applications Soc. Ann. Meeting*, pp. 366–382, 1976.
[10] J. Sun, "Impedance-Based Stability Criterion for Grid-Connected Inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3075–3078, Nov. 2011.
[11] X. Zhou, L. Zhou, Y. Chen, Z. Shuai, J. M. Guerrero, A. Luo, W. Wu, and L. Yang, "Robust Grid-Current-Feedback Resonance Suppression Method for LCL-Type Grid-Connected Inverter Connected to Weak Grid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 2126–2137, 2018.
[12] L. Jia, X. Ruan, W. Zhao, Z. Lin, and X. Wang, "An Adaptive Active Damper for Improving the Stability of Grid-Connected Inverters Under Weak Grid," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9561–9574, Nov. 2018.
[13] J. Xu, B. Zhang, and S. Xie, "Stability and Improvement of LCL-Filtered Inverters Using only Grid Current Feedback Active Damping for Weak Grid Applications," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 3301–3306, Mar. 2018.
[14] X. Zhang, X. Danni, F. Zhichao, G. Wang, and D. Xu, "An Improved Feedforward Control Method Considering PLL Dynamics to Improve Weak Grid Stability of Grid-Connected Inverters," *IEEE Transactions on Industry Applications*, pp. 5143 – 5151, 2018.
[15] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.
[16] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of phase-locked loop low-frequency stability in three-phase grid-connected power converters considering impedance interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310–321, Jan. 2015.
[17] T. Thacker, R. Burgos, F. Wang, and D. Boroyevich, "Single-phase islanding detection based on phase-locked loop stability," in *2009 IEEE Energy Conversion Congress and Exposition*, pp. 3371–3377, Sep. 2009.
[18] J. Xu, Q. Qian, and S. Xie, "Adaptive control method for enhancing the stability of grid-connected inverters under very weak grid condition," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1141–1146, Mar. 2018.
[19] "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," *IEEE Std 1547-2003*, pp. 1–28, Jul. 2003.
[20] K. Zhou, Z. Qiu, N. R. Watson, and Y. Liu, "Mechanism and elimination of harmonic current injection from single-phase grid-connected PWM converters," *IET Power Electronics*, vol. 6, no. 1, pp. 88–95, Jan. 2013.
[21] Z. Xin, P. Mattavelli, W. Yao, Y. Yang, F. Blaabjerg, and P. C. Loh, "Mitigation of Grid-Current Distortion for LCL-Filtered Voltage-Source Inverter With Inverter-Current Feedback Control," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6248–6261, Jul. 2018.
[22] J. He, B. Liang, Y. W. Li, and C. Wang, "Simultaneous Microgrid Voltage and Current Harmonics Compensation Using Coordinated Control of Dual-Interfacing Converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2647–2660, Apr. 2017.
[23] T. Abeyasekera, C. M. Johnson, D. J. Atkinson, and M. Armstrong, "Suppression of line voltage related distortion in current controlled grid connected inverters," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1393–1401, Nov. 2005.
[24] X. Wang, D. Yang, and F. Blaabjerg, "Harmonic current control for LCL-filtered VSCs connected to ultra-weak grids," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 1608–1614, Oct. 2017.
[25] S. Buso, T. Caldognetto, and Q. Liu, "Analysis and Experimental Characterization of a Large-Bandwidth Triple-Loop Controller for Grid-Tied Inverters," *IEEE Transactions on Power Electronics*, pp. 1936 – 1949, 2019.
[26] T. Caldognetto, Q. Liu, and S. Buso, "Self-tuning of triple-loop controlled grid-connected inverters," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 7121–7127, Sep. 2018.
[27] P. Mattavelli, "An improved deadbeat control for UPS using disturbance observers," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 206–212, Feb. 2005.
[28] C. Zhang, X. Wang, and F. Blaabjerg, "Analysis of phase-locked loop influence on the stability of single-phase grid-connected inverter," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–8, Jun. 2015.
[29] J. Xu, Q. Qian, and S. Xie, "Adaptive control method for enhancing the stability of grid-connected inverters under very weak grid condition," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1141–1146, Mar. 2018.
[30] A. Adib, B. Mirafzal, X. Wang, and F. Blaabjerg, "On Stability of Voltage Source Inverters in Weak Grids," *IEEE Access*, vol. 6, pp. 4427–4439, 2018.
[31] A. Khodamoradi, G. Liu, P. Mattavelli, T. Caldognetto, and P. Magnone, "Analysis of an On-Line Stability Monitoring Approach for DC Microgrid Power Converters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2018.
[32] R. Teodorescu, M. Liserre, and P. Rodríguez, *Grid Converters for Photovoltaic and Wind Power Systems*. Wiley, 2011.
[33] S. Moon, L. Corradini, and D. Maksimović, "Autotuning of digitally controlled boost power factor correction rectifiers," *IEEE Transactions on Power Electronics*, vol. 26, no. 10, pp. 3006–3018, Oct. 2011.

Qing Liu (S'18) received the B.S. and M.S. degrees in electrical engineering from the School of Automation, Northwestern Polytechnical University, China, in 2012 and 2015, respectively. She is currently a Ph.D. student of power electronics with the Department of Information Engineering (DEI) at the University of Padova, Italy. Her main research interests are in the fields of low-voltage microgrids, nano-grids and are particularly related to digital control of power electronic converters.

Tommaso Caldognetto (S'10-M'16) received the M.S. (Hons.) degree in electronic engineering and the Ph.D. degree in information engineering from the University of Padova, Italy, in 2012 and 2016, respectively. In 2014, he was a visiting Ph.D. student with the Institute for Automation of Complex Power Systems, University of Aachen, Germany. He is currently a researcher with the Department of Technology and Management, University of Padova. His research interests include control of grid-tied converters, microgrid architectures, and real-time simulation for power electronics.

Simone Buso (M'97) received the M.Sc. degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padova, Italy, in 1992 and 1997, respectively. He is currently an Associate Professor of electronics with the Department of Information Engineering (DEI) at the University of Padova. His main research interests are in the industrial and power electronics fields and are related specifically to switching converter topologies, digital control of power converters, renewable energy sources and smart micro-grids.