Supplementary Information

An integrated CMOS quantitative-polymerase-chain-reaction lab-on-chip for point-of-care diagnostics

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Electrowetting droplet transport on the surface of a CMOS IC

Supplementary Video 1 shows the actuation of a 1.2-nL droplet between adjacent pixels in the array. This movement is used to characterize actuation voltages under different surface and temperature conditions. Supplementary Video 2 shows the actuation of a larger 3-nL droplet across the entire surface of the electrowetting array.

Post-processing of the CMOS integrated circuit to define the electrowetting region

A detailed process diagram showing the post-processing steps to define the electrowetting region is given in Figure S-1.1. Prior to encapsulation, excess polyimide and silicon nitride is removed from the edges of the surface glass cut using a 10 minute nitric acid soak. The chip is mounted on and signal paths wirebonded to a BGA-272 package (Figure S-1.2). A PEN dam is mounted on the BGA-272 in order to contain the poured SU-8(Figure S-1.3)

The BGA package is heated to 70°C in order to decrease SU-8 viscosity upon contact with the heated substrate. The SU-8 is poured directly from the bottle in order to minimize air bubbles. On a level hotplate (Electronic Micro Systems 1000-1), we slowly ramp the temperature of the SU8 on the package from room temperature to 65°C and hold for 30 minutes. The temperature is then increased from 65°C to 95°C and held for 8.5 hours. The pre-bake concludes with a decrease ramp from 95°C to 25°C for the final 30 minutes. An SU-8 long-pass filter is used on the Karl Suss MA-6 mask aligner. Exposure is 6000mJ at 10mW. The sample is immediately placed on a room temperature hotplate and slowly ramped to 75°C over 5min. The sample temperature is held steady at 75°C for 25 minutes after which it is slowly cooled to room temperature over a span of 20 minutes. The device is soaked in 5mL of SU-8 Developer for 30 minutes. Stir agitation is provided using a magnetic stir bar at 60 rpm. The sample is first rinsed in isopropanol and then with water. Aspect ratios of 10:1 have been demonstrated with this recipe for SU-8 thickness ranging from 500µm to 2mm. Figure S-1.4 illustrates fully patterned SU-8 on the chip surface. Wirebonds have been encapsulated and the electrowetting active region exposed with use of SU-8.

Following the SU-8 patterning, a conformal coating of Parylene-C is deposited atop the chip surface to provide adequate dielectric isolation. Total thickness of the Parylene-C layer is 2µm. Deposition is performed using the Labcoter2 Parylene Deposition Chamber (Specialty Coating Services; Indianapolis, Indiana). To increase the hydrophobicity of the dielectric layer, a 100nm thick layer of Teflon AF (DuPont, New York, New York) spin coated atop the Parylene-C. A volume of 10µL of Teflon® AF amorphous fluoroplastic resin in solution (6%WT) is added to the reservoir. The spin profile is as follows: Spin at 1500rpm for 45 seconds. The Teflon is baked at 125°C for 75 seconds. Final stack is shown in Figure S-1.5.

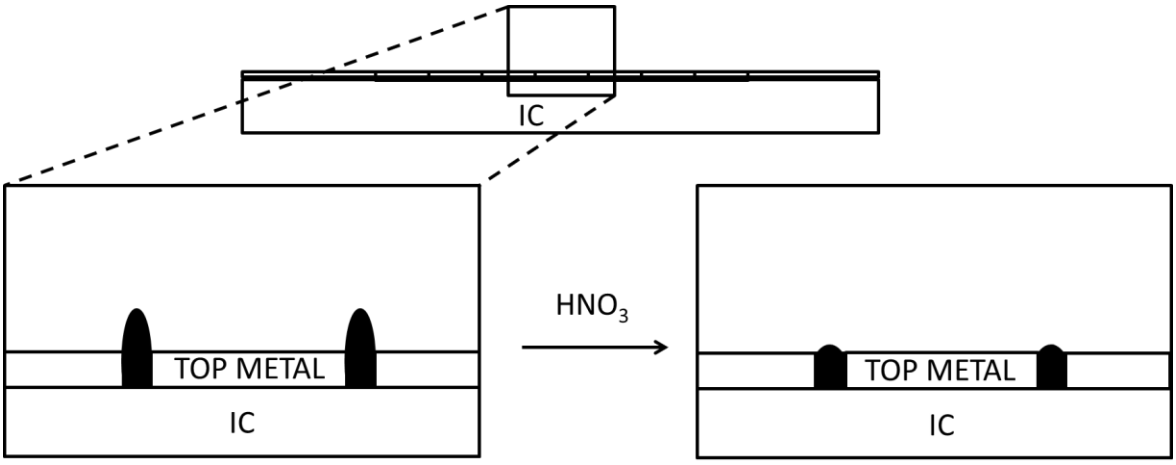

Figure S-1.1: Nitric acid passivation etch to remove polyimide and silicon nitride

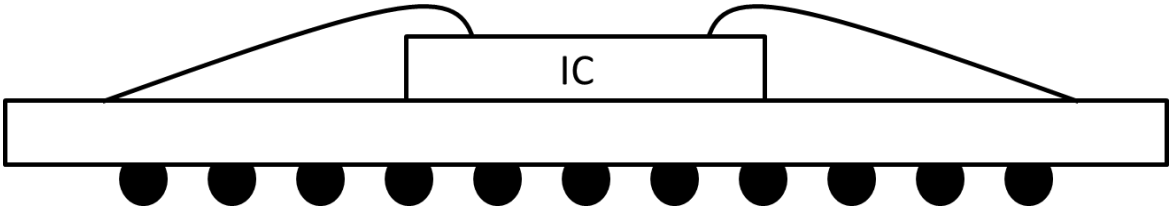

Figure S-1.2: Wirebonding the IC to the BGA 272 package

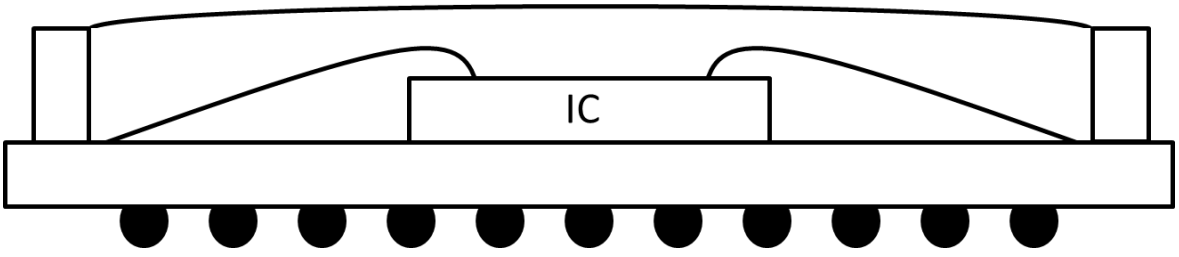

Figure S-1.3: SU-8 2100 application around wirebonded IC bounded by a PEN guard ring

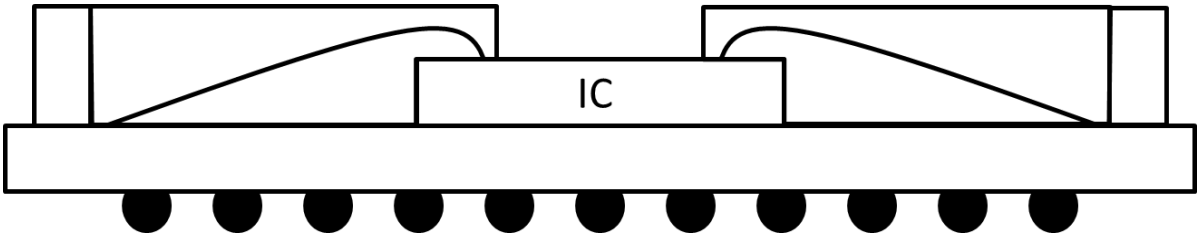

Figure S-1.4: Fully patterned SU-8; wirebonds protected while center of chip is exposed

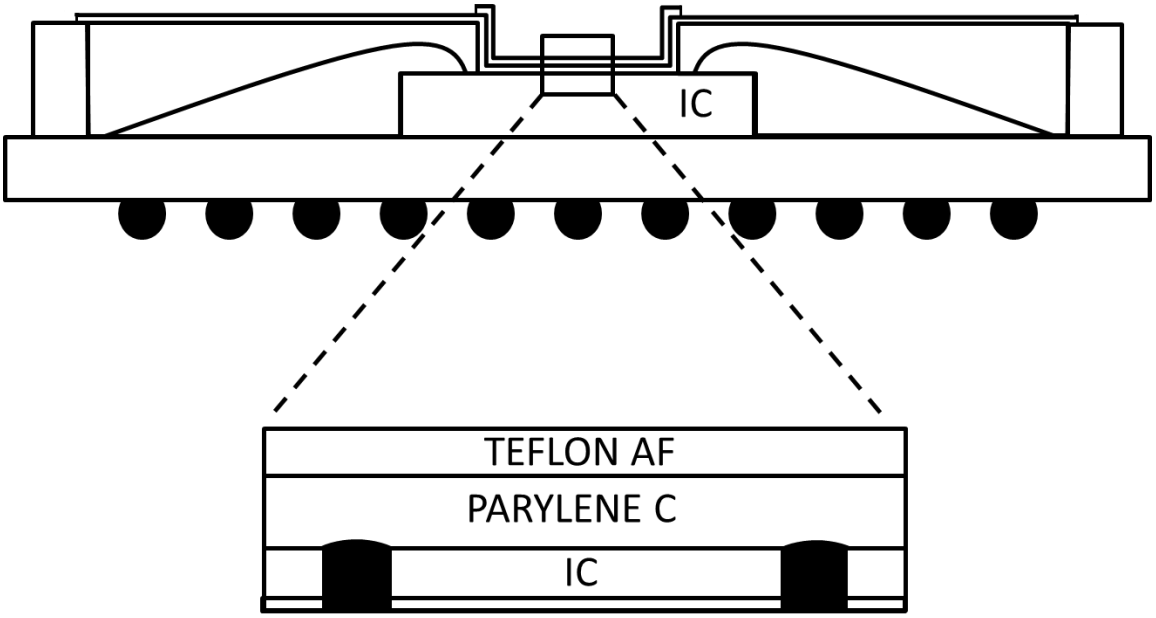

Figure S-1.5: Final stack with Parylene C (thermal evaporation) and Teflon AF (spin-coated)