SIS3316 Family

16 Channel VME Digitizer

16 Channel Desktop Digitizer

GL ISO 9001

GL Systems Certification

SIS3316 Digitizer Boards

SIS3316-125-16 125 MSPS 16-bit

SIS3316-250-14 250 MSPS 14-bit

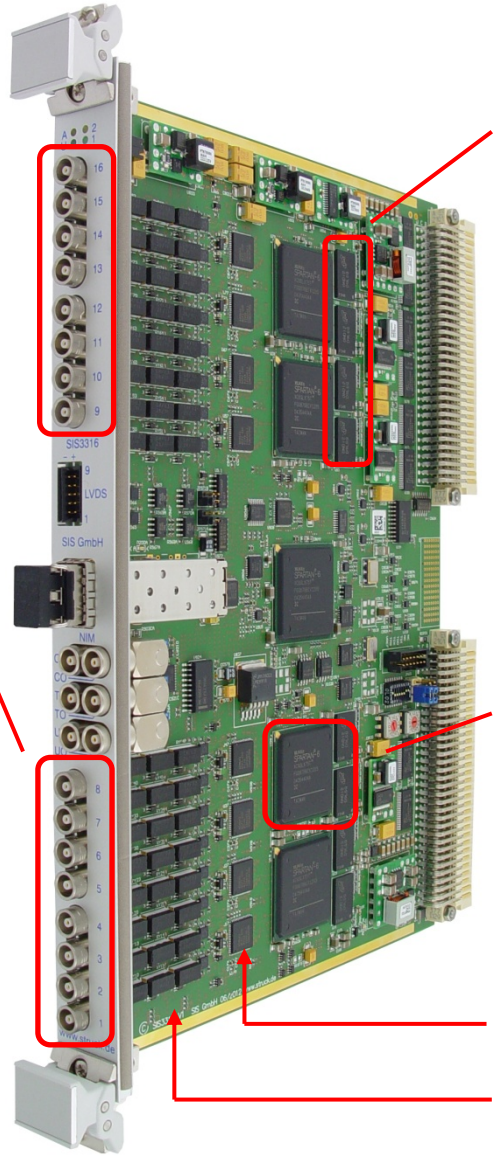
SIS3316 16 channel VME FADC

16 Analog Input Connectors

- Programmable Input Termination
• 50 Ohm
• High Impedance

- Programmable Input Range
• 5V
• 2V

- Programmable Analog Offset (DAC)
-> variable Input Range from +5V/0V to 0V/-5V
-> variable Input Range from +2V/0V to 0V/-2V



DDR3 Memory

4 x 2 x 256 MByte = 2GByte

• 512 MByte / 4-channel group
• 128 MByte / channel

• 64 MSample / channel

ADC FPGA: Xilinx Spartan 6

XC6SLX75T-3
-compatible options:
* XC6SLX100T
* XC6SLX150T

Application Firmware

250 MSPS 14-bit ADC or
125 MSPS 16-bit ADC

Impedance/Range Relays
and Offsets (DACs)

Frontpanel BLVDS Bus

- Clock distribution
- Sample control
- Trigger
- Timestamp clear
- …….

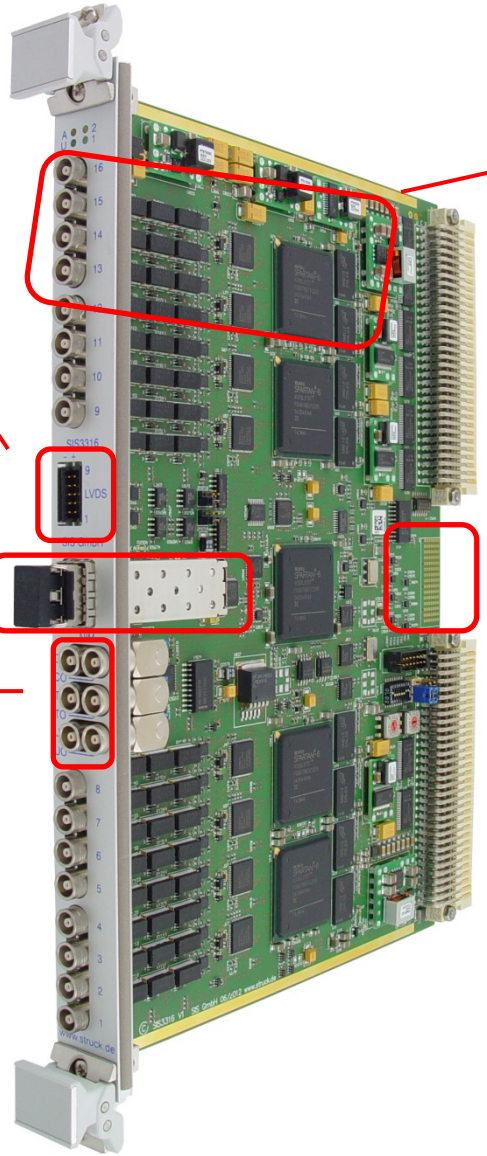
SFP Cage

- Gigabit Ethernet
- Multi-Gigabit optical link connection

NIM Control In/Output

- 3 Inputs
- Input 1:
  sample clock or firmware dependant function
- Inputs 2/3:
  function firmware dependant

- 3 Outputs
- Output 1/2/3:
  function firmware dependant



4 channel ADC group

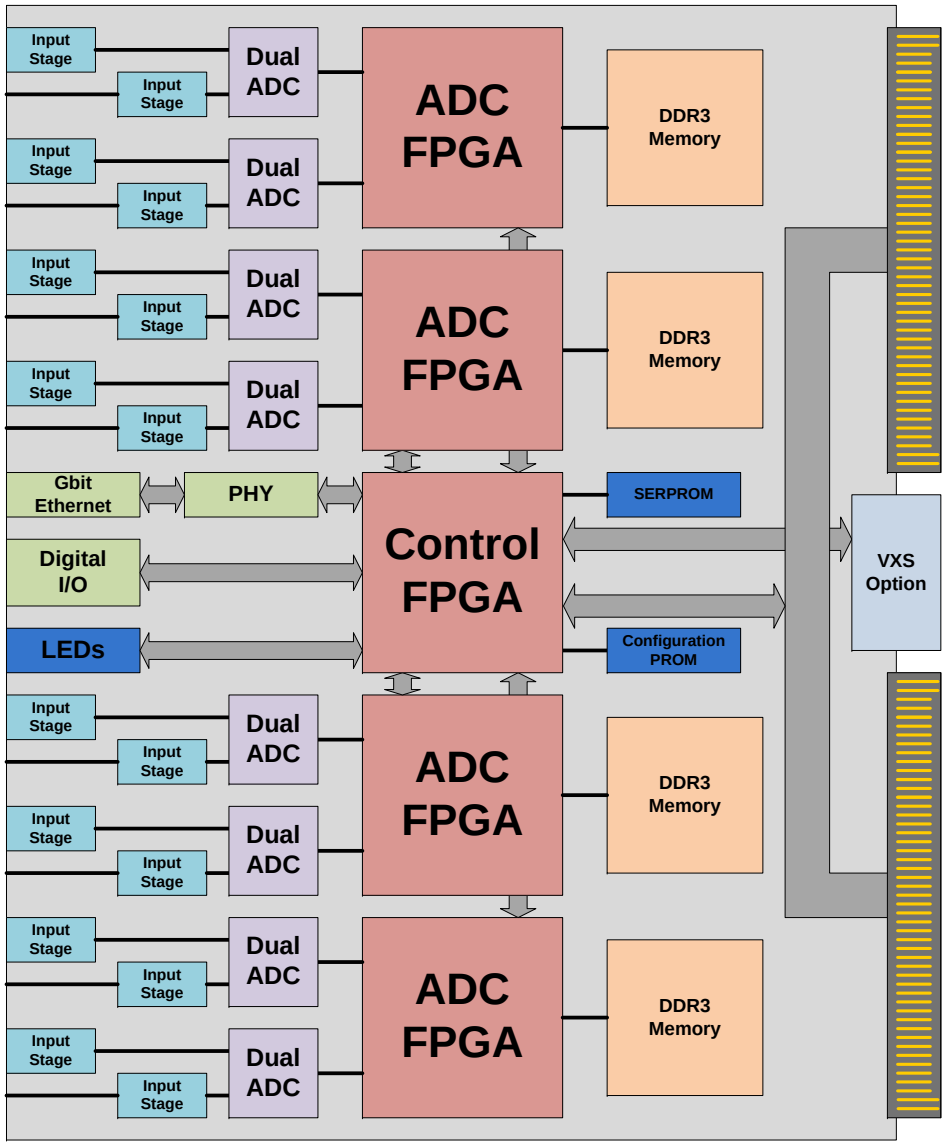
- 4 channel inputs
- 1 Spartan 6 FPGA
- 512 MByte DDR3 memory

VXS connector space

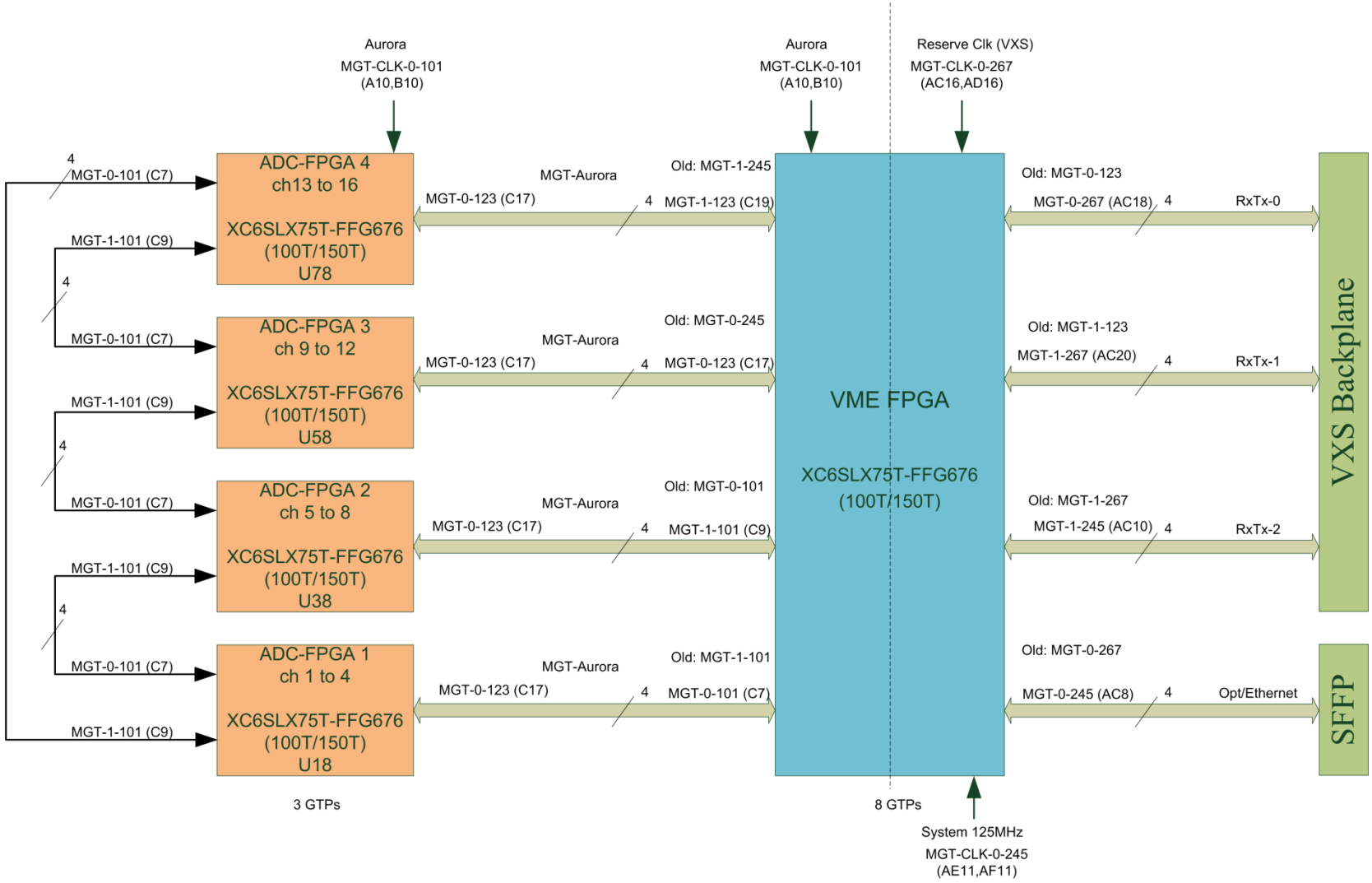
SIS3316 Desktop Digitizer

Gbit/s Ethernet or Optical Link Readout

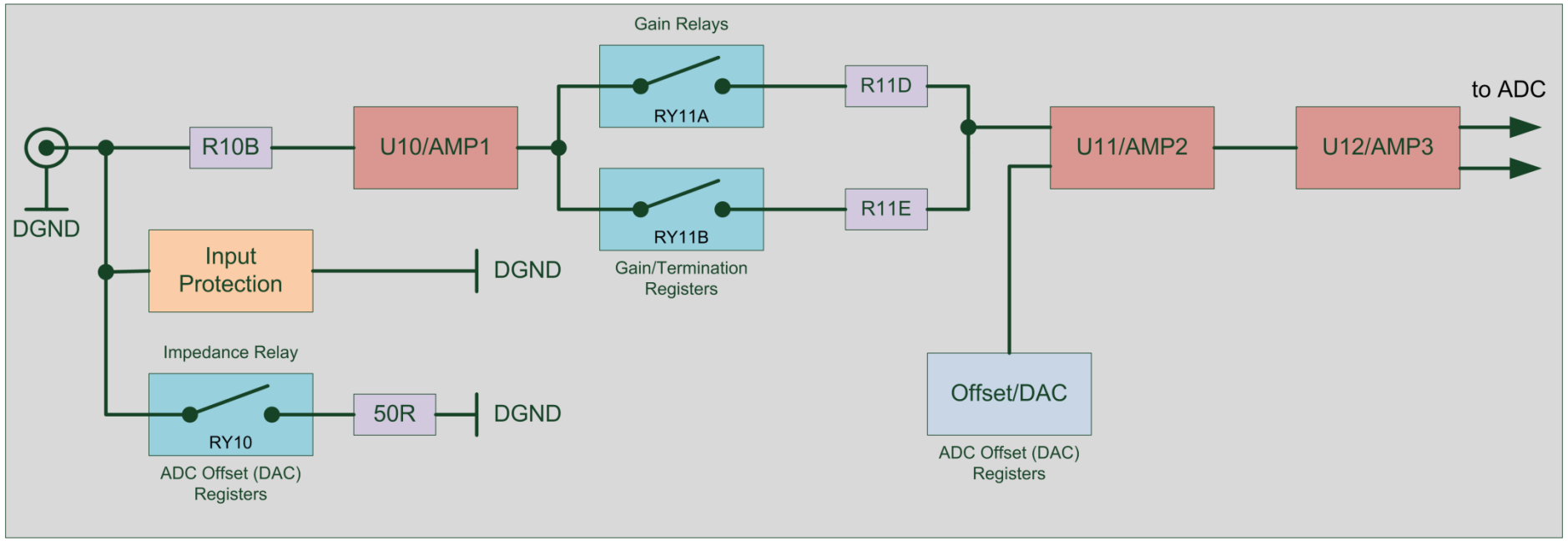
SIS3316 Block Diagram



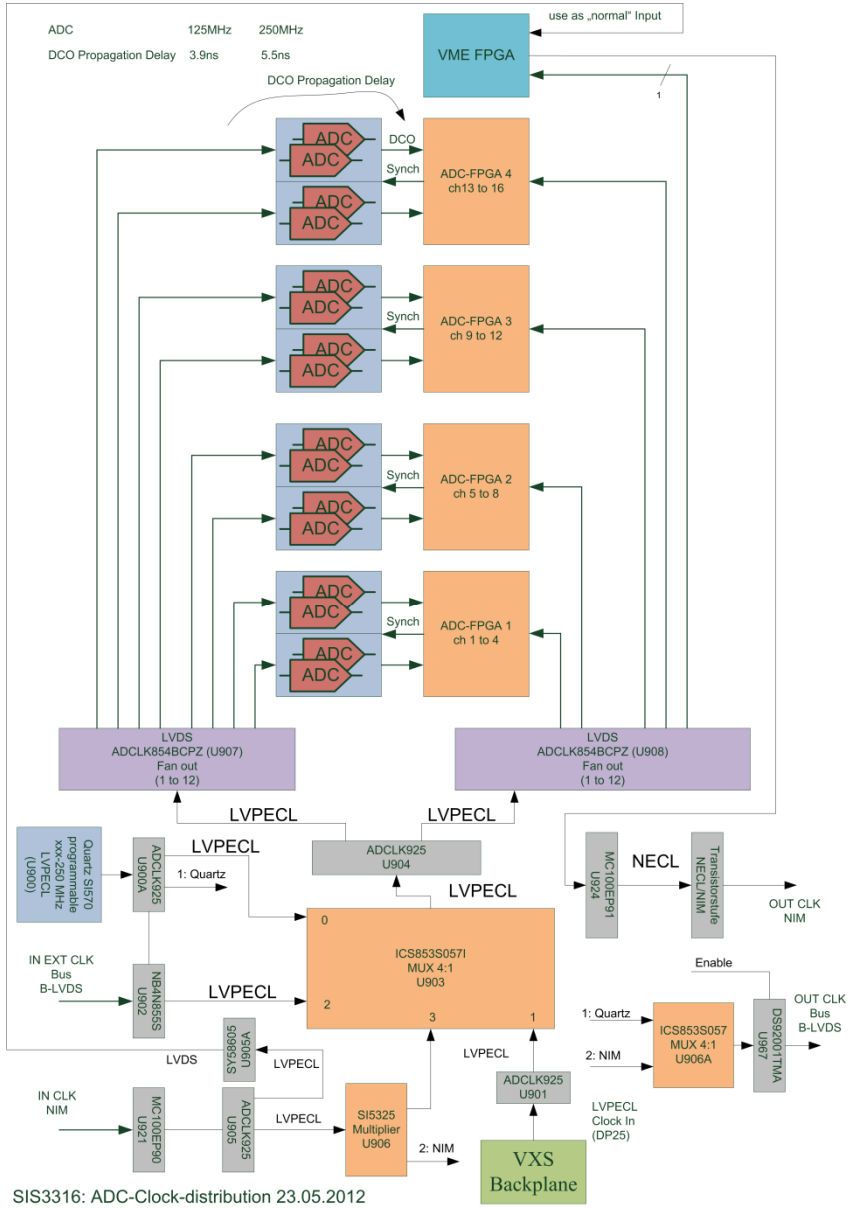
SIS3316 MGT-Links connections



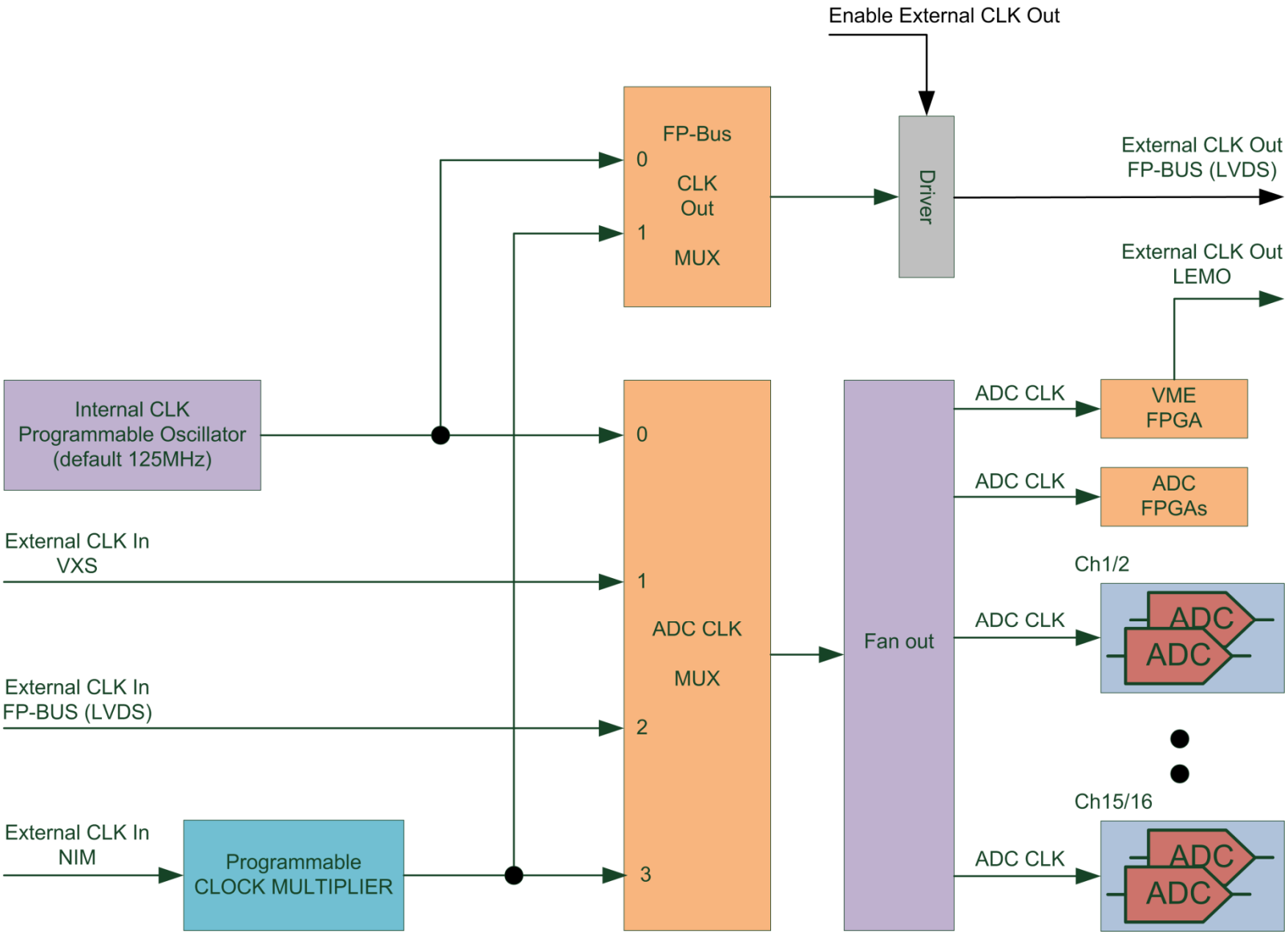
SIS3316 Analog Input Stage



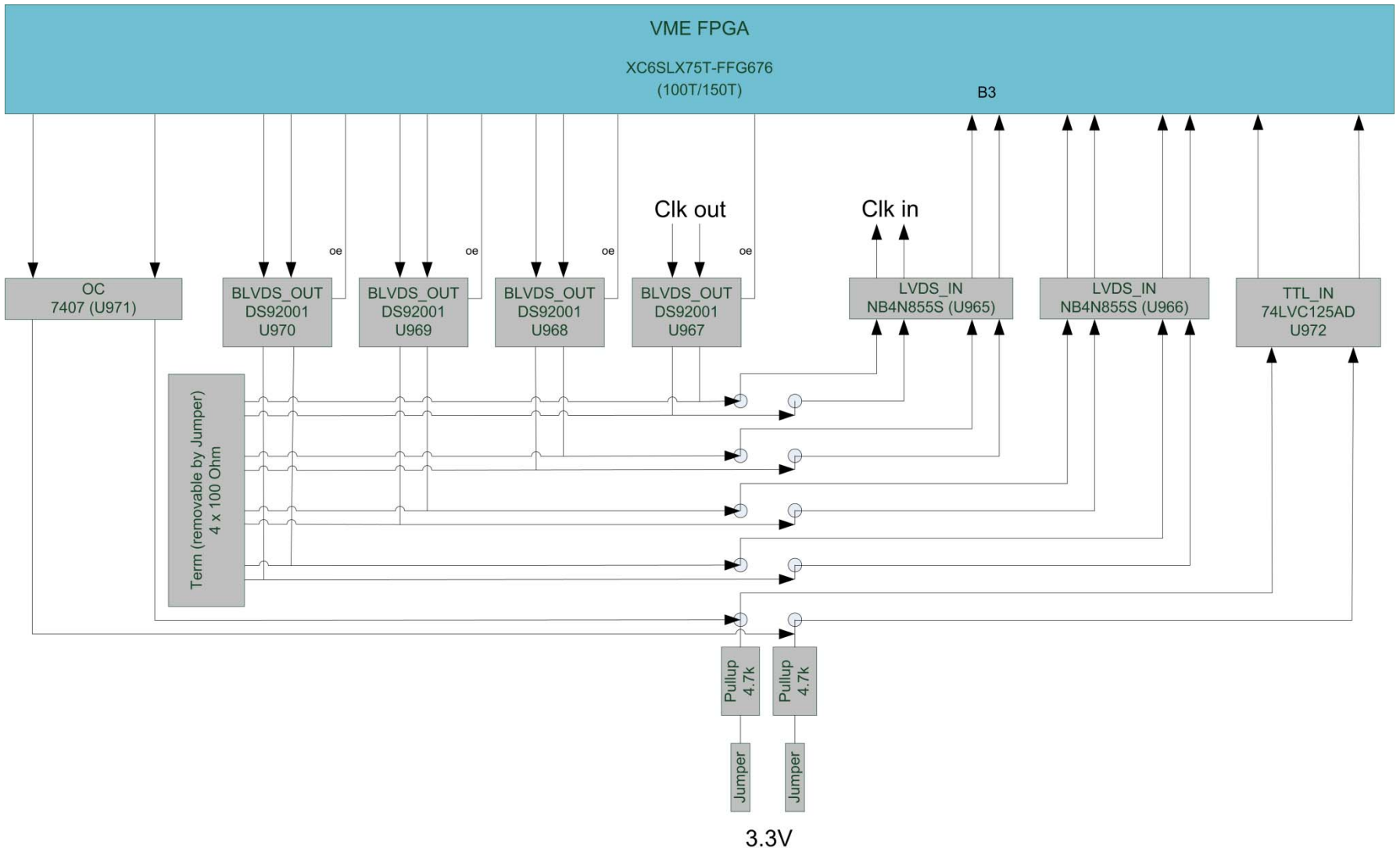
SIS3316 Sample Clock distribution



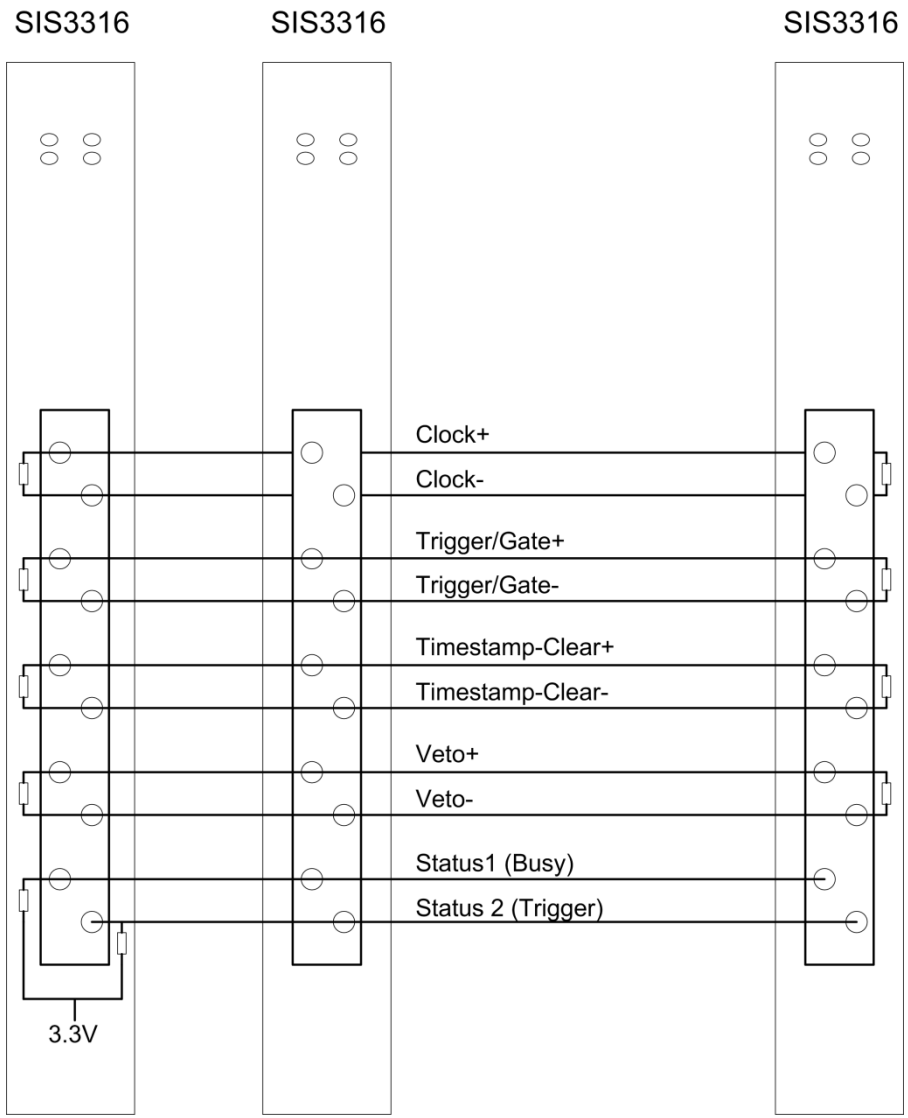
SIS3316 Sample Clock programming



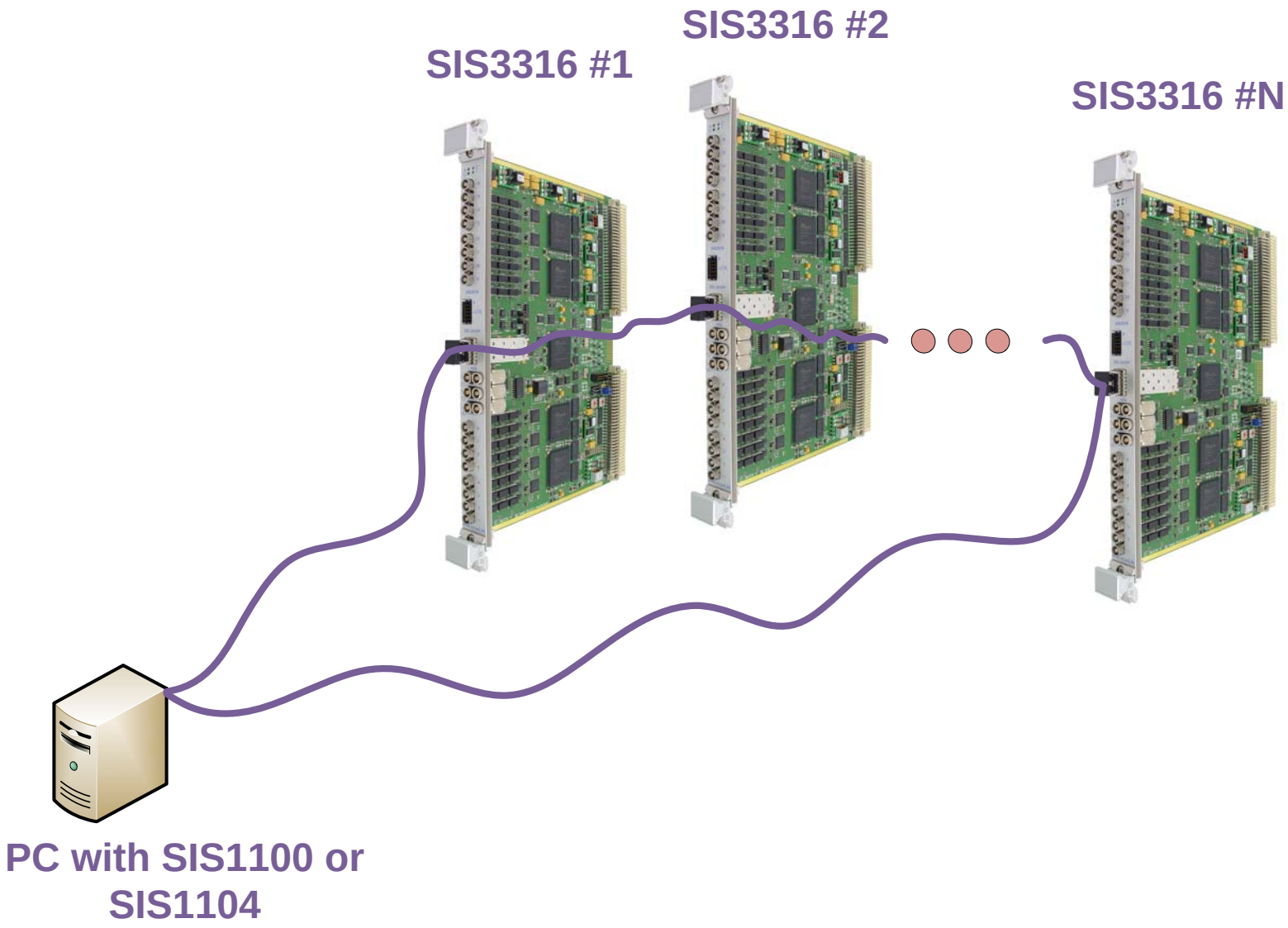
SIS3316 Frontpanel BLVDS-Bus



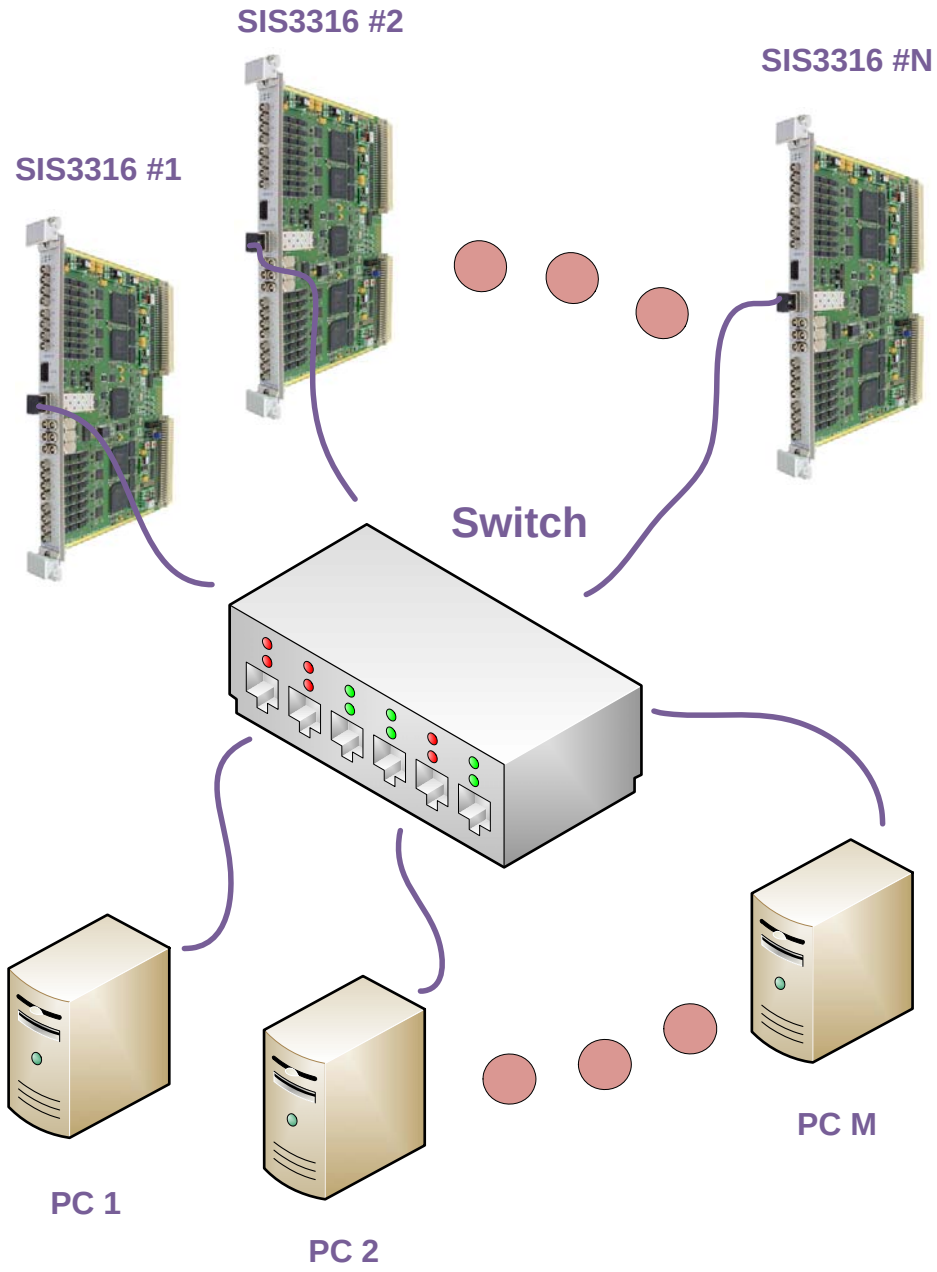
Frontpanel BLVDS-Bus application example



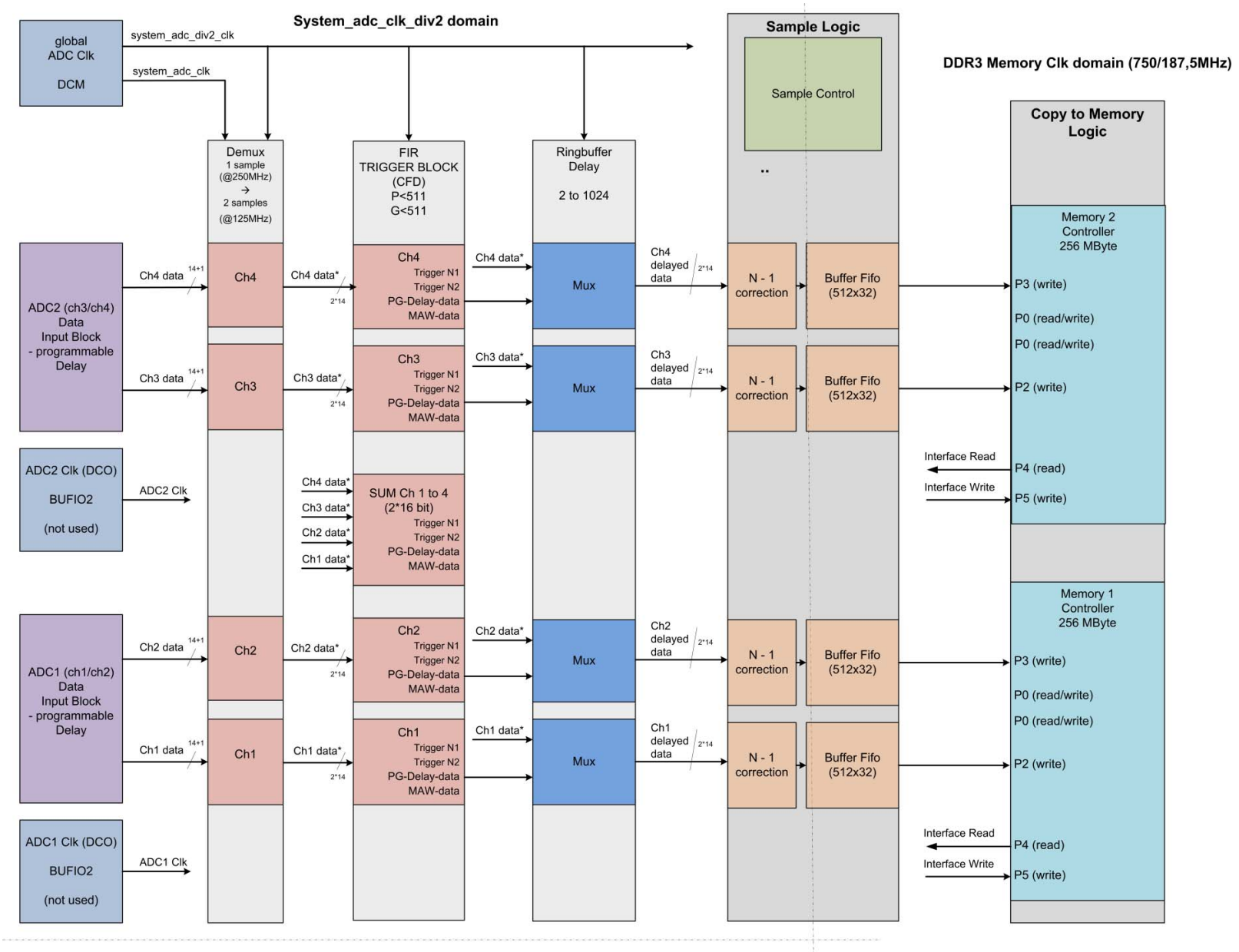
SIS3316 readout with optical fiber ring
#03145 FTLF8524P2BNV



SIS3316 readout with Ethernet
#04333 FCLF-8520-3



ADC FPGA Firmware Implementation



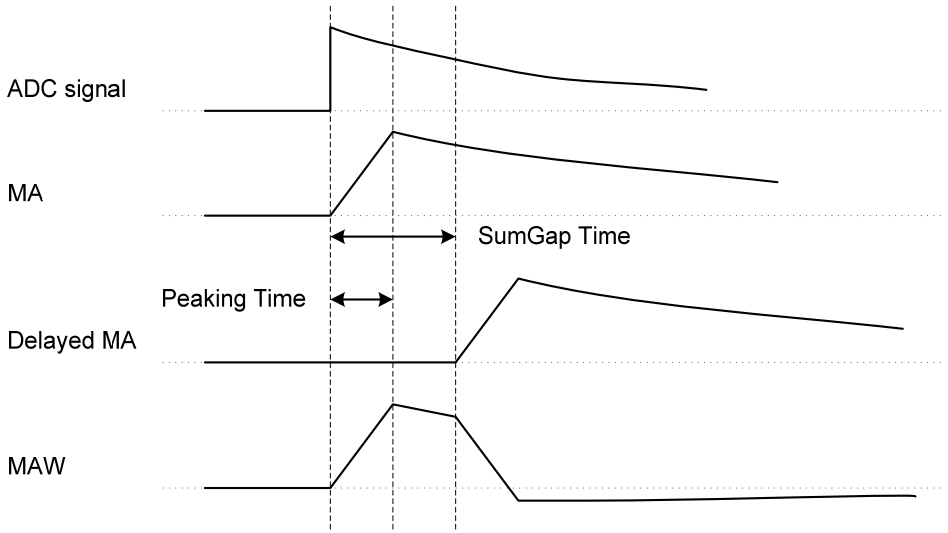
Trigger: Trapezoidal FIR Filter

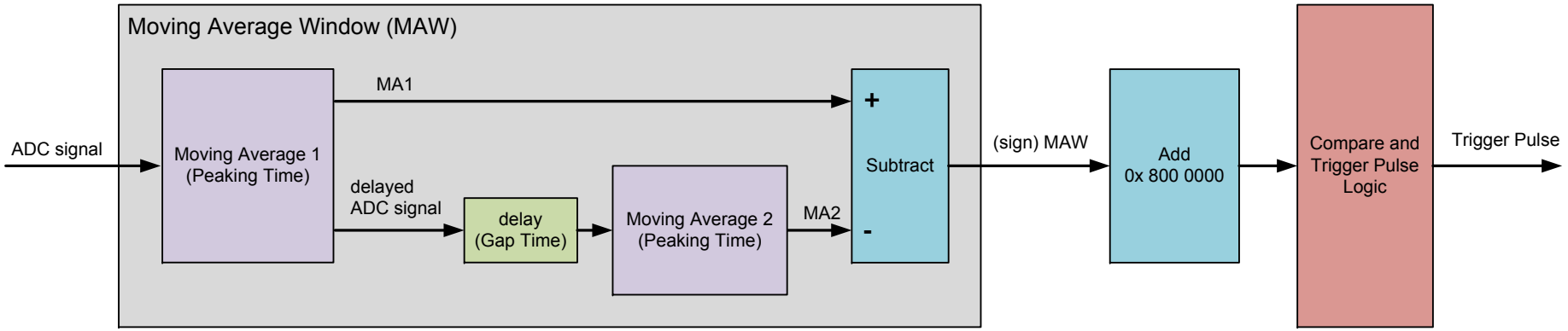
- A trapezoidal FIR filter is implemented for each ADC Channel to generate a trigger signal.

Features for each ADC channel:

- Programmable Peaking Time (max. 510 Clocks)
- Programmable Gap Time (max. 510 Clocks)
- Programmable Trigger Threshold
- Programmable CFD Mode
- Programmable Trigger Mode (GT,Disable)

Implementation



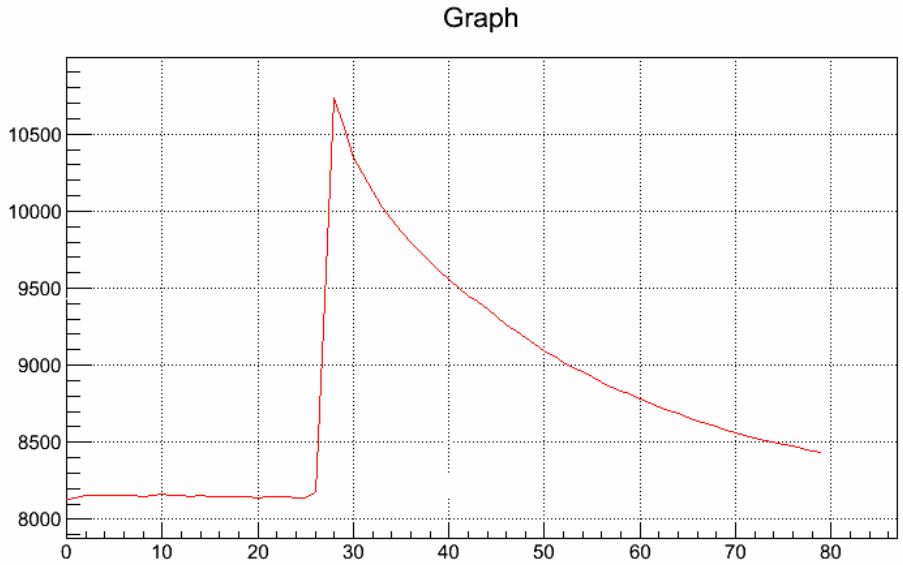


Explanation:

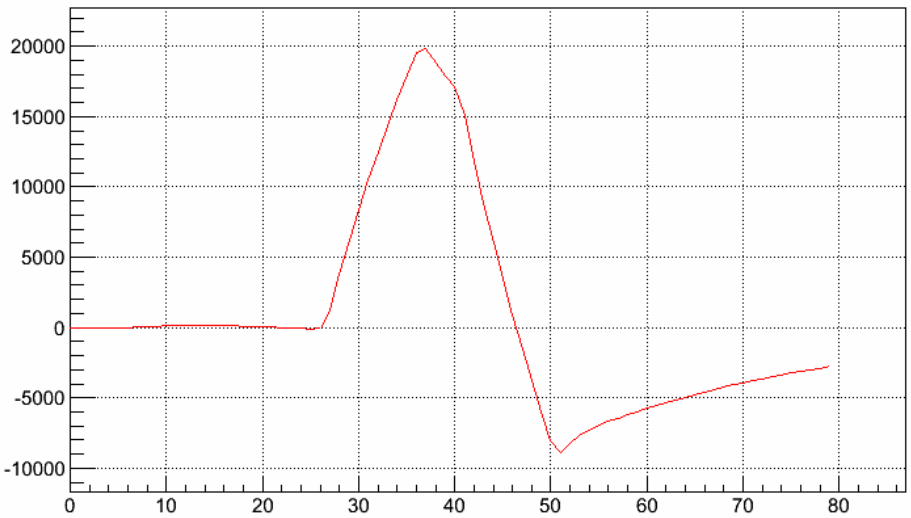
•MAW:	moving average window
•MA:	moving average
•Decimation:	decreasing the clock rate
•Peaking Time:	the length of the MA for moving average unit
•SumGap Time:	the differentiation time of the moving window average unit

Illustration with Signal

Raw Signal

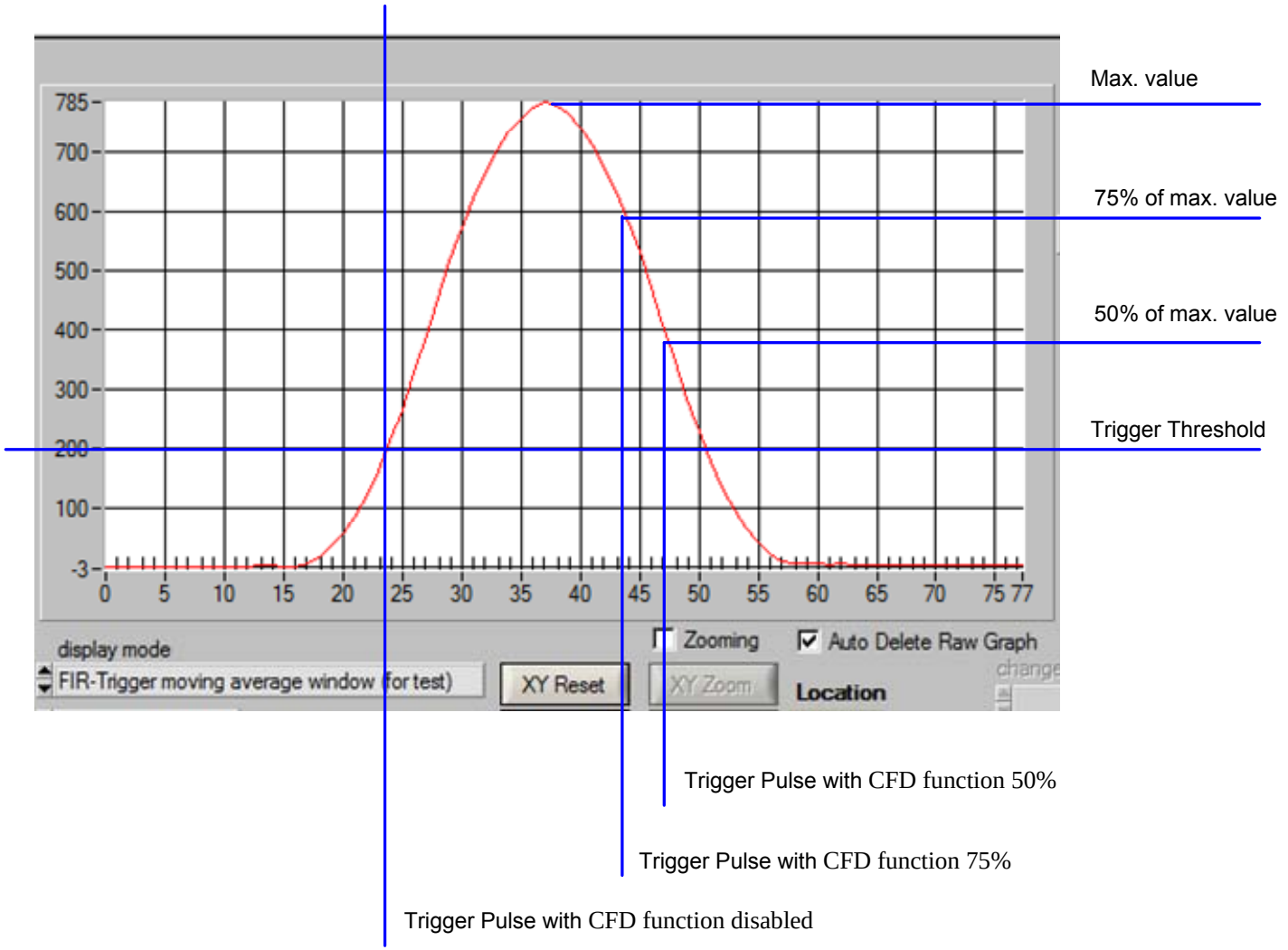


MAW Trapezoidal:
P = 10, G = 4

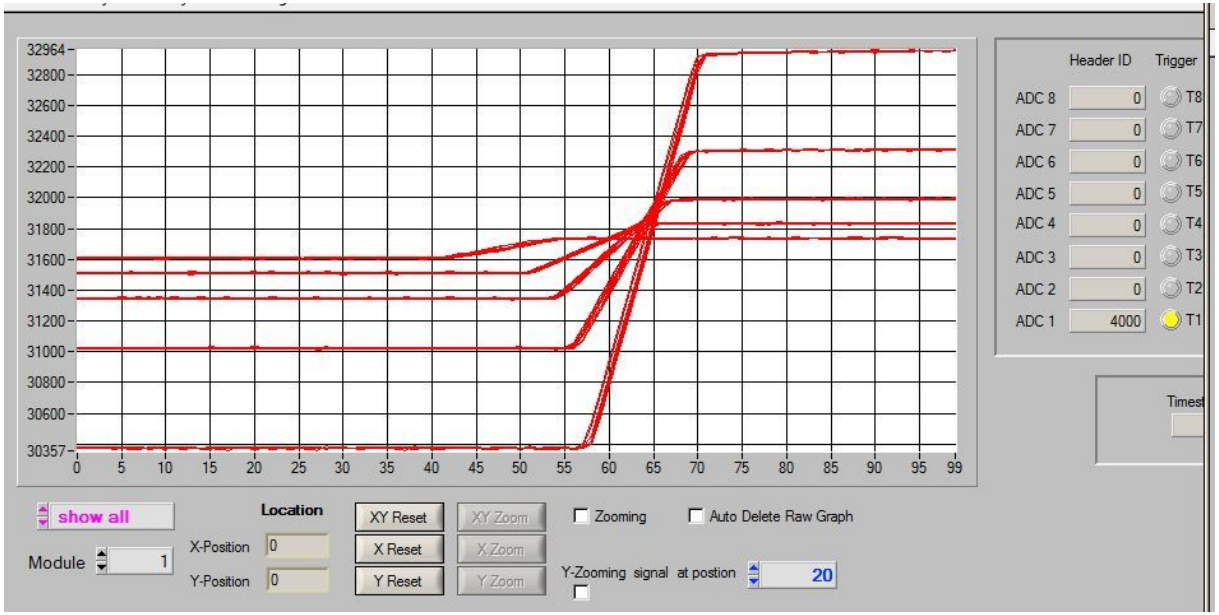


Firmware: CFD Trigger

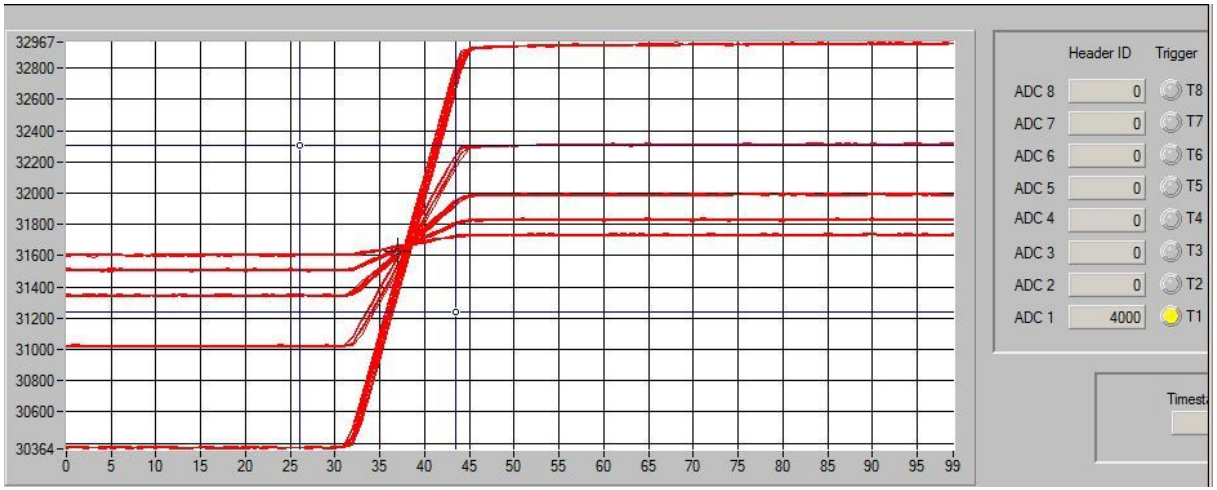
P = 10, G = 10 (sumG = 20)
Signal rise time 100ns



CFD Trigger disabled



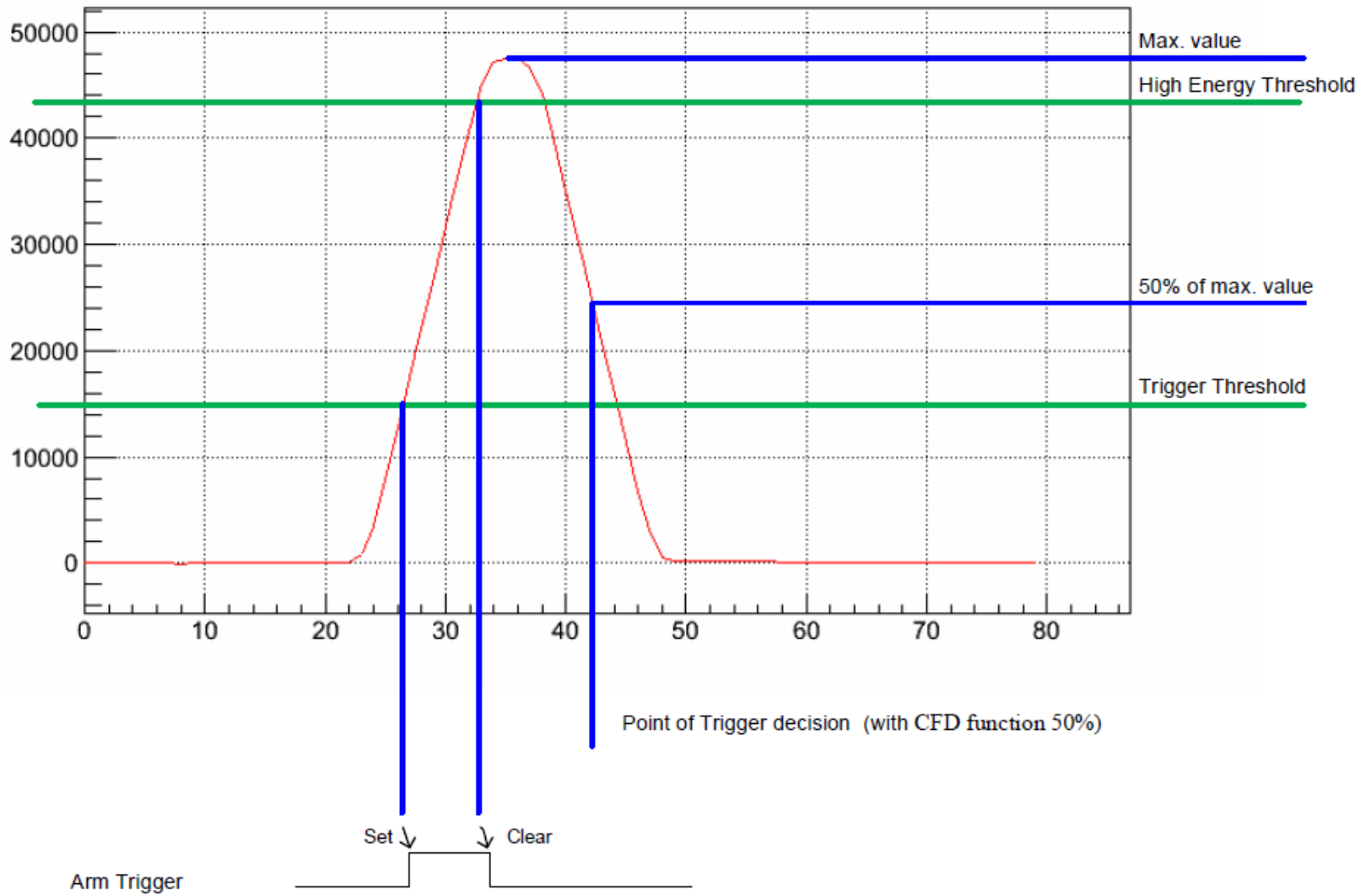
CFD Trigger enabled



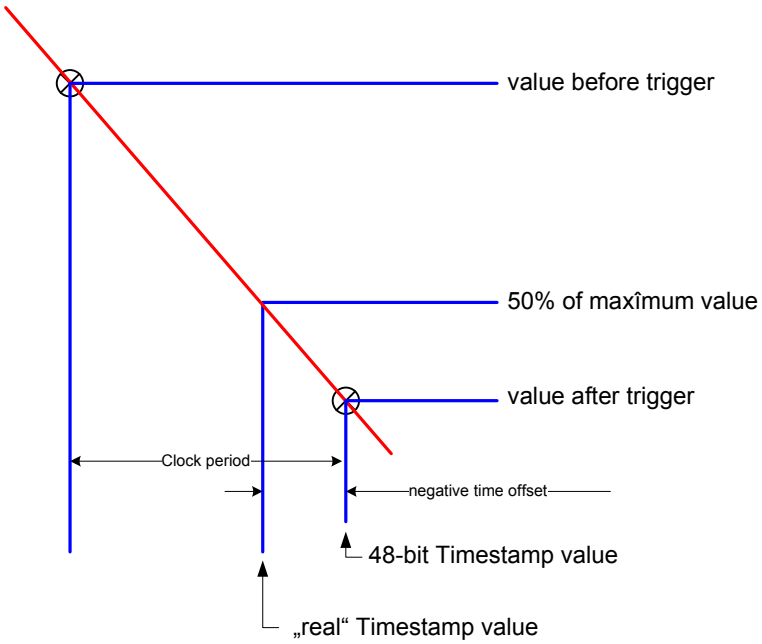
Hi Energy Trigger Supression

P = 10, G = 4

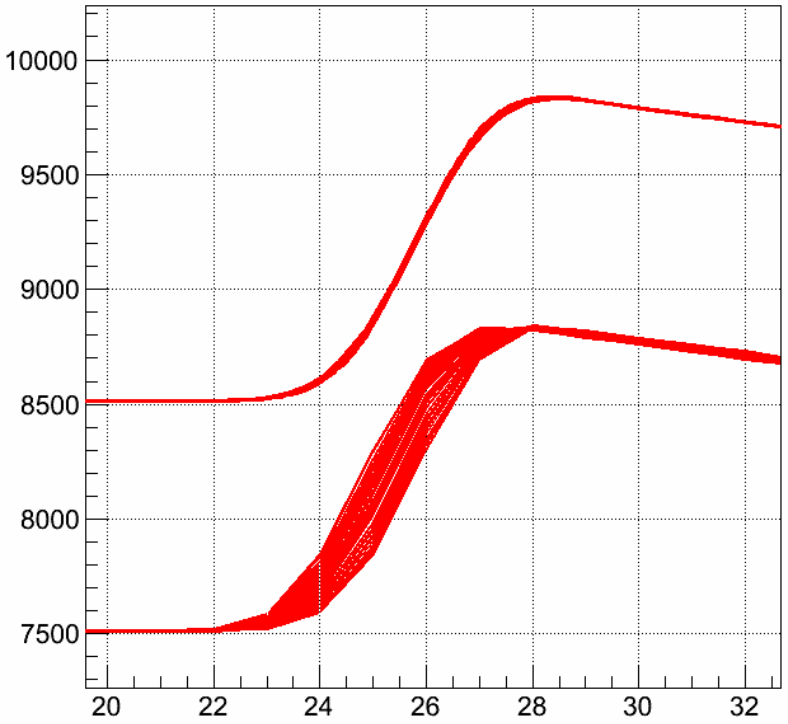
Signal rise time 10ns



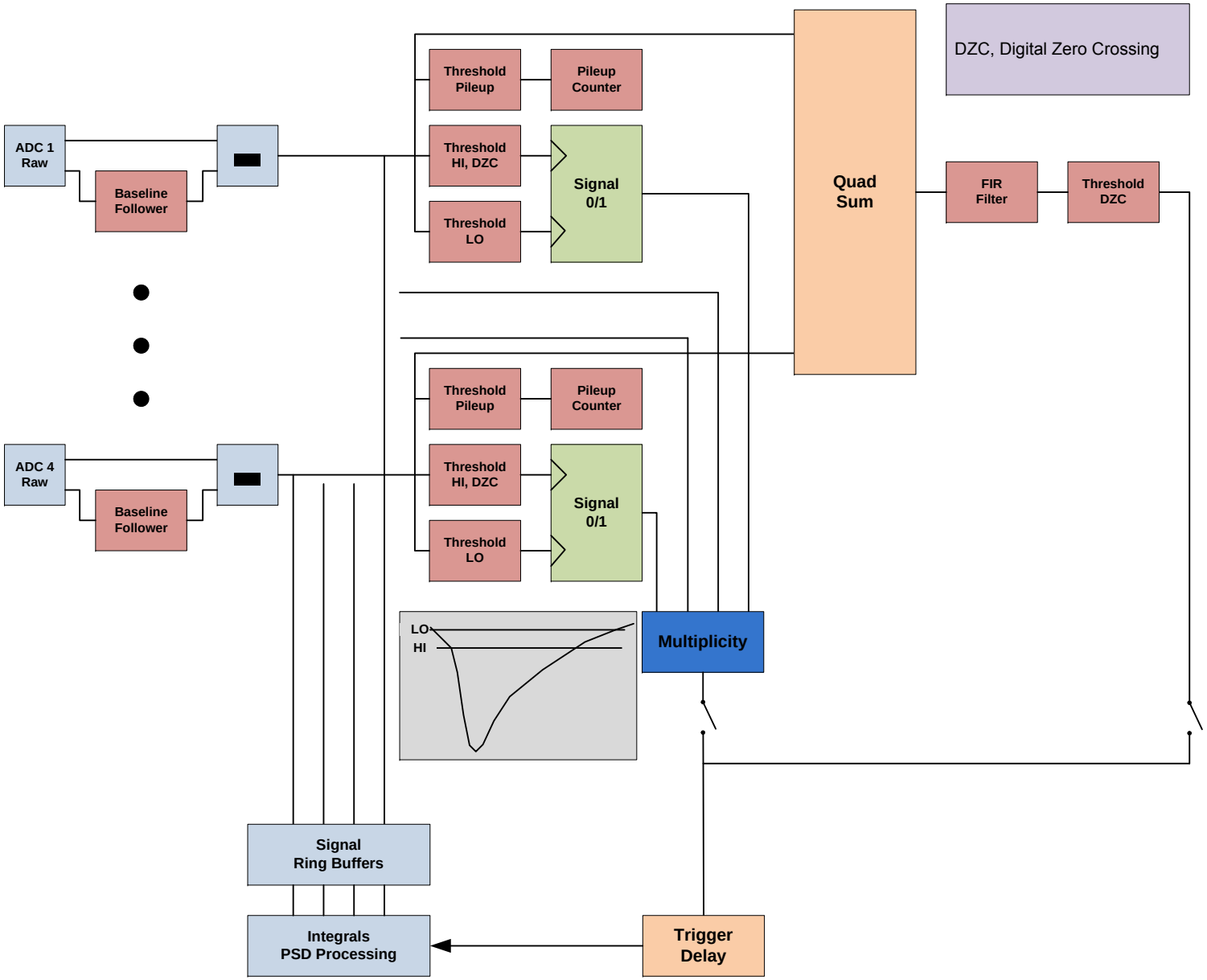
Firmware Highlights
Subsample Time Resolution



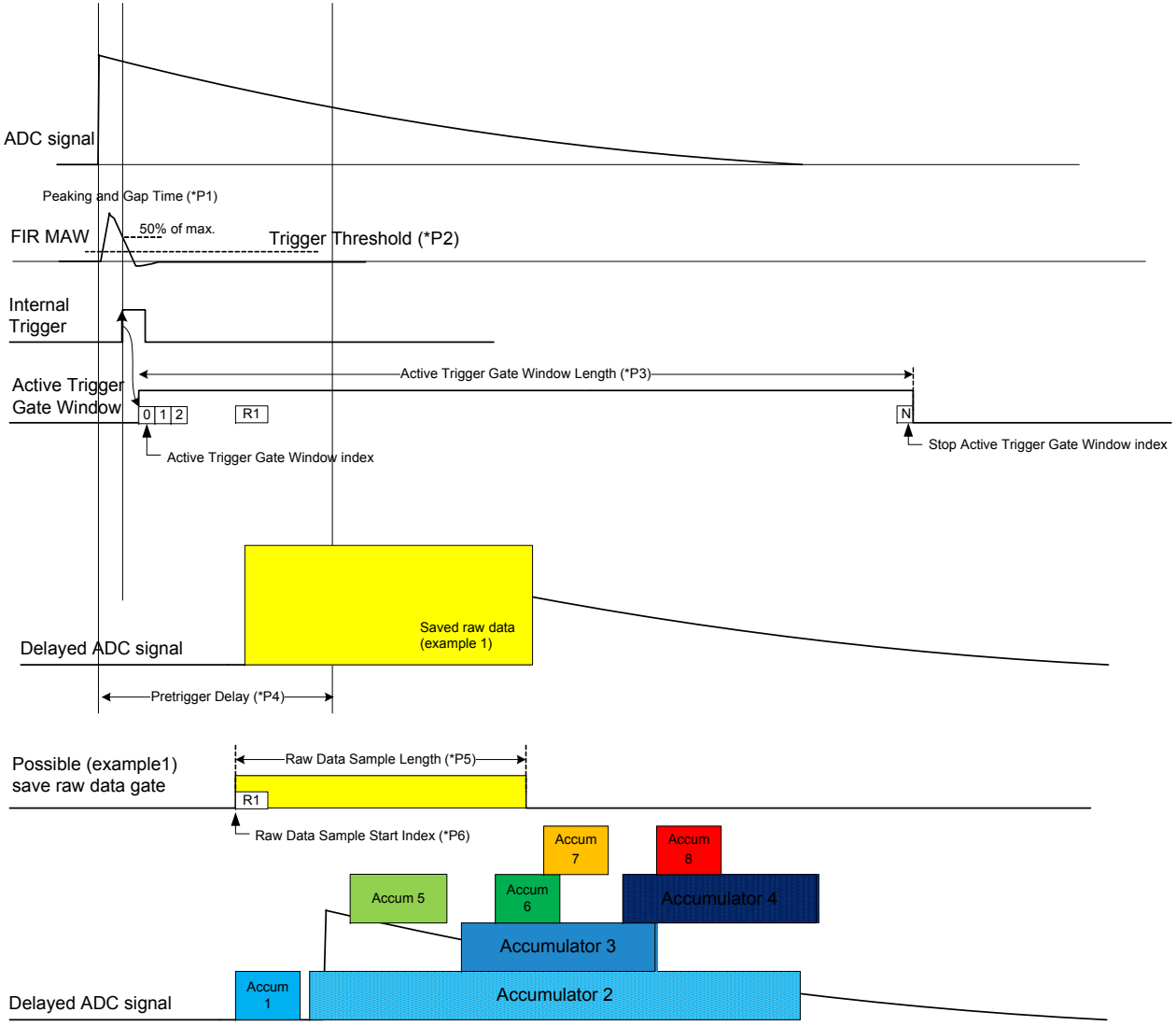
Corrected (upper traces) and raw (lower traces)
→ resolution < 70 ps



Firmware 4 Channel Sum Trigger

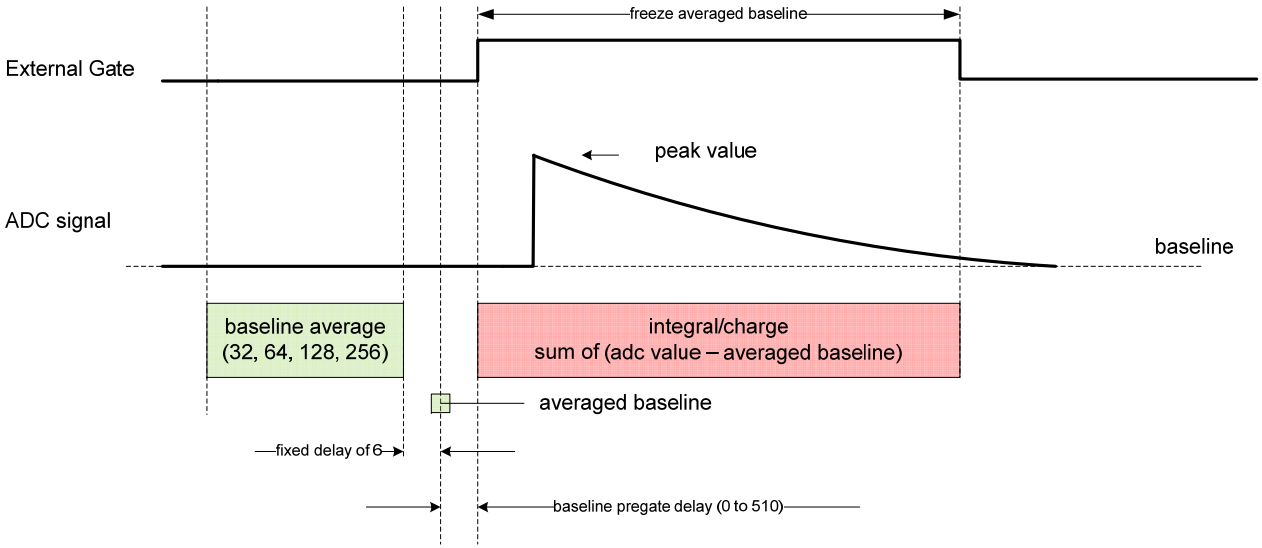


Firmware Highlights
n/Gamma Implementation



Firmware Highlights
Peak/Charge ADC Implementation

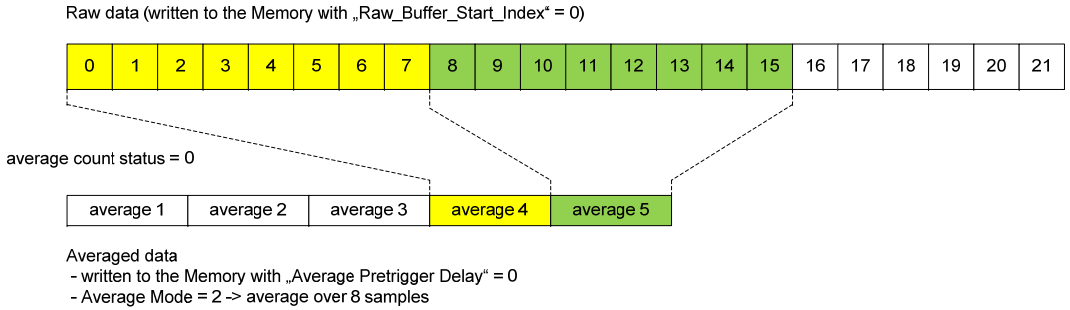
This mode is available starting with ADC firmware version 0x02500005.
An external gate (connected to front panel input TI) is used to define the area in which the signal maximum (peak height) and the charge are computed. The averaged baseline is subtracted in both cases. The baseline average can be 32, 64, 128 or 256 samples long (defined by the two baseline average mode bits) and the baseline pregate delay defines how many samples ahead of the leading edge of the gate the moving baseline average is frozen and stored to the event header. A fixed delay of 6 samples has to be taken into account as shown below.

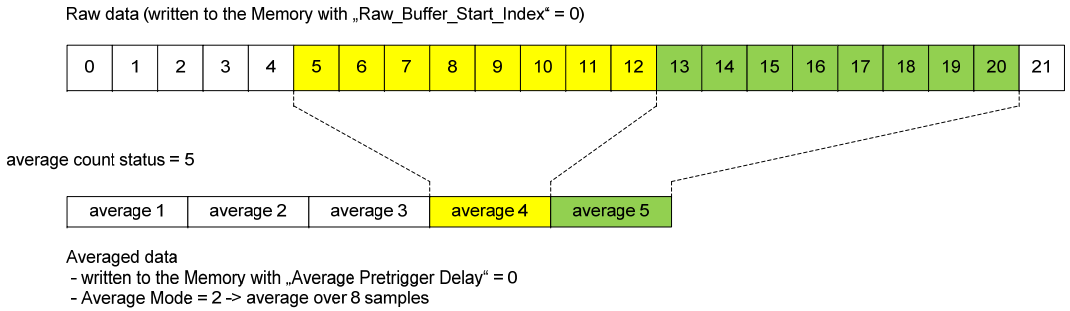


Firmware Highlights
Averaging Mode Implementation I

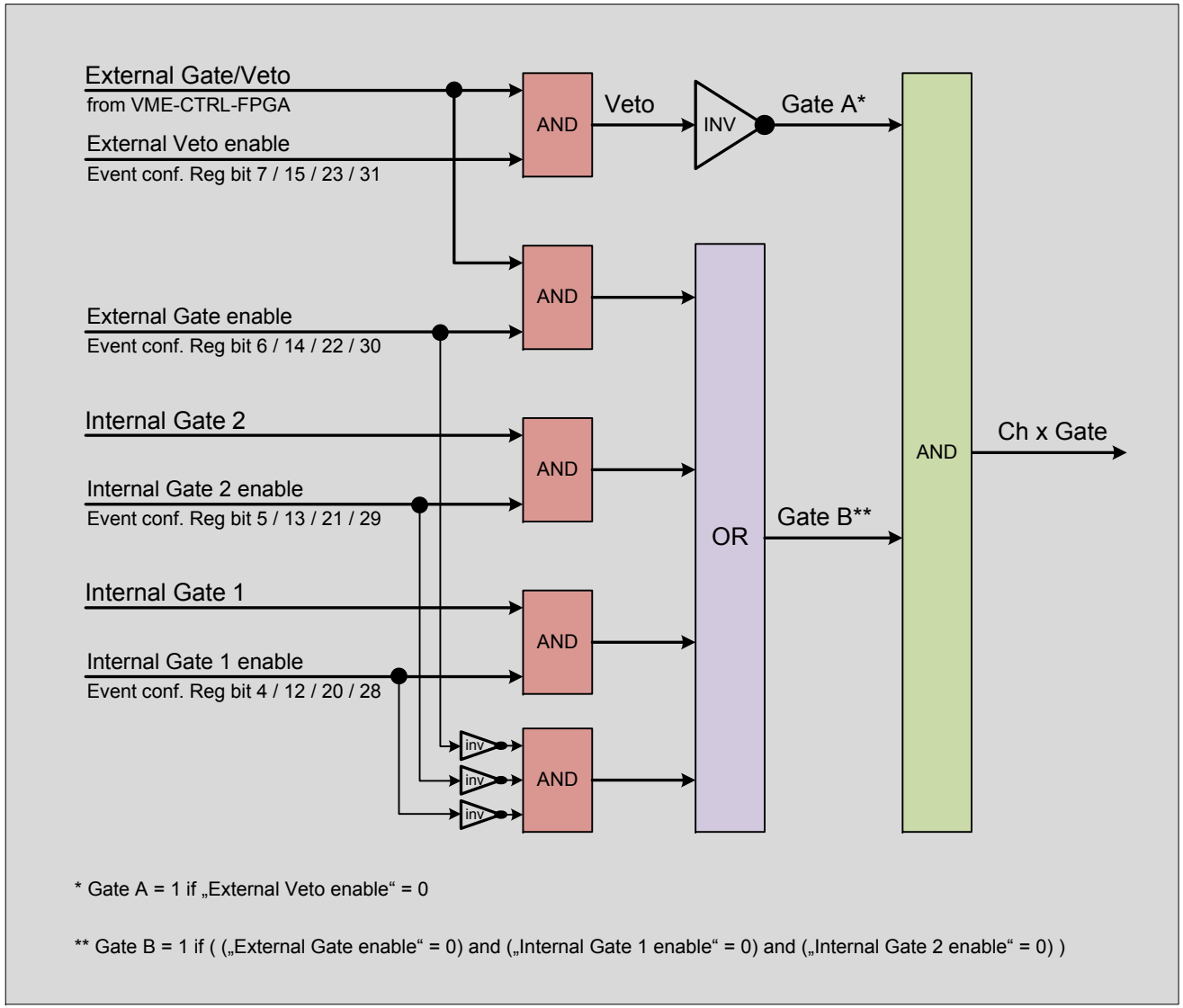
Averaging mode is available starting with ADC firmware version 0x02500004. Originally this mode was implemented for the maXs (Micro-Calorimeter Arrays for High Resolution X-ray Spectroscopy) application. You can average 4, 8, 16, 32, 64, 128 or 256 samples (defined by the setting of the three average mode bits), program a 12-bit wide average pretrigger delay and define a 16-bit wide number of averaged samples (average sample length) to be aqcuired. The internal clock range from 10 MHz to 125 MHz corresponds to a sampling speed of some 40 KSPS to 500 KSPS in combination with 256 sample averaging. The average count status information in the data allows for timing of the first sample of the first averaged value relative to the trigger as illustrated below. The averaged values are shifted to 16-bit to enable storage of two averaged samples in one 32-bit data word.
Especially with a higher number of samples to be averaged, the effective number of bits (ENOB) is virtually equal to the nominal number of bits.

Firmware Highlights
Averaging Mode Implementation II





Firmware Highlights
Coincidence Logic



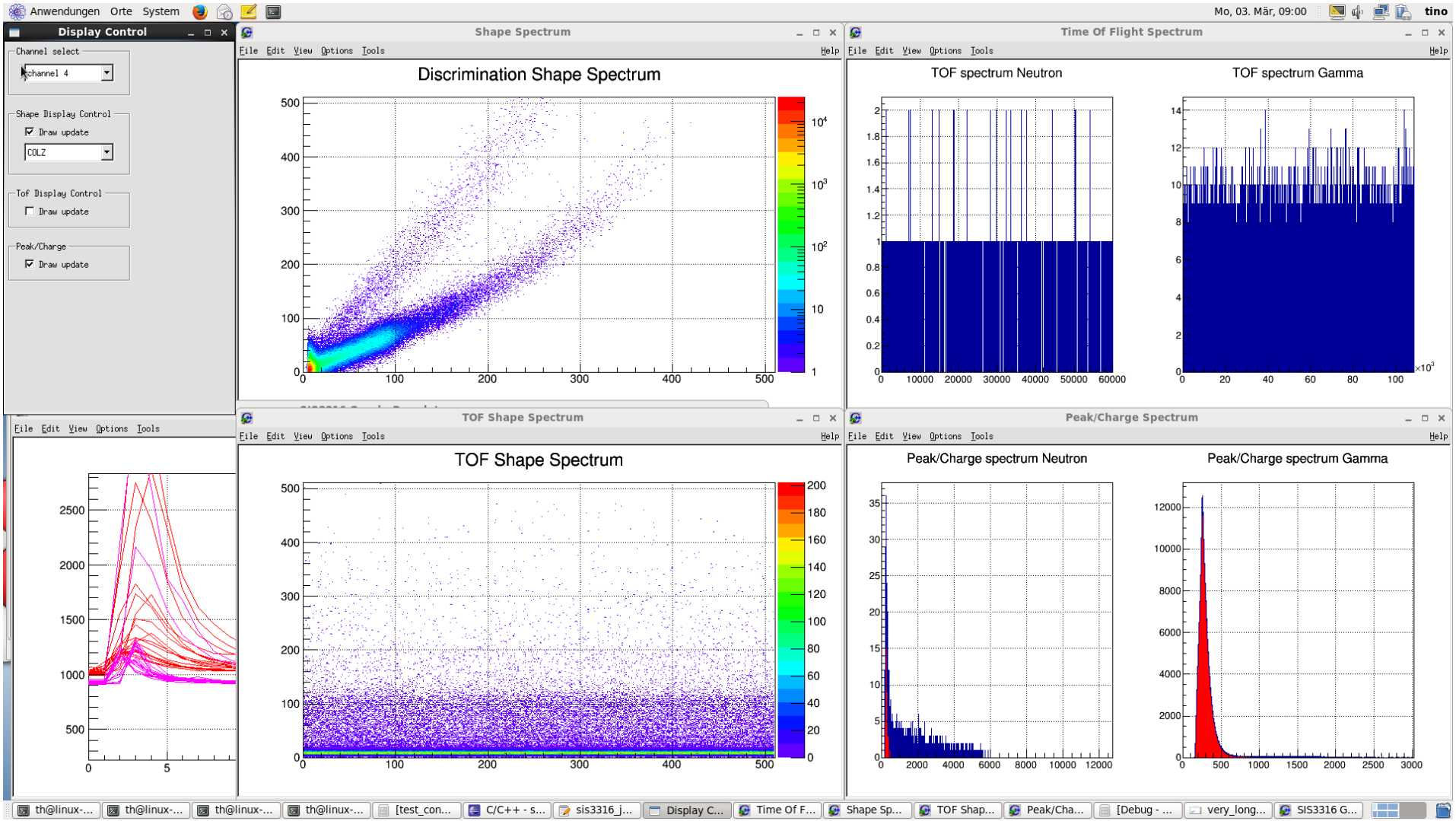
* Gate A = 1 if „External Veto enable“ = 0

** Gate B = 1 if ((„External Gate enable“ = 0) and („Internal Gate 1 enable“ = 0) and („Internal Gate 2 enable“ = 0))

Custom Firmware Example n/Gamma w. TOF Histogramming

- Double Bank / Multi event operation
- 16 channel asynchronous (internal trigger generation) and synchronous (external trigger, global trigger) operation
- Internal Trigger generation for each channel (FIR filter with CFD feature, baseline independent)
- 3 Accumulators/Integrals (1 x 24-bit, 2 x 28-bit) for each channel
- Peak height finder
- Baseline determination
- 32-bit Timestamp
- Flexible Hit/Event storage (additional raw data, FIR Trigger trapezoidal MAW values)
- Internal TOF (time of flight) 1D-Histograms (up to 1M Histogram, two histograms per channel)
- Internal Shape 2-D Histograms (up to 512 x 512 Histogram, two histograms per channel)
- Internal Peak-Height/Charge 1-D Histograms (up to 1K (64K) Histogram, two histograms per channel)
- Beam On/Off separation feature

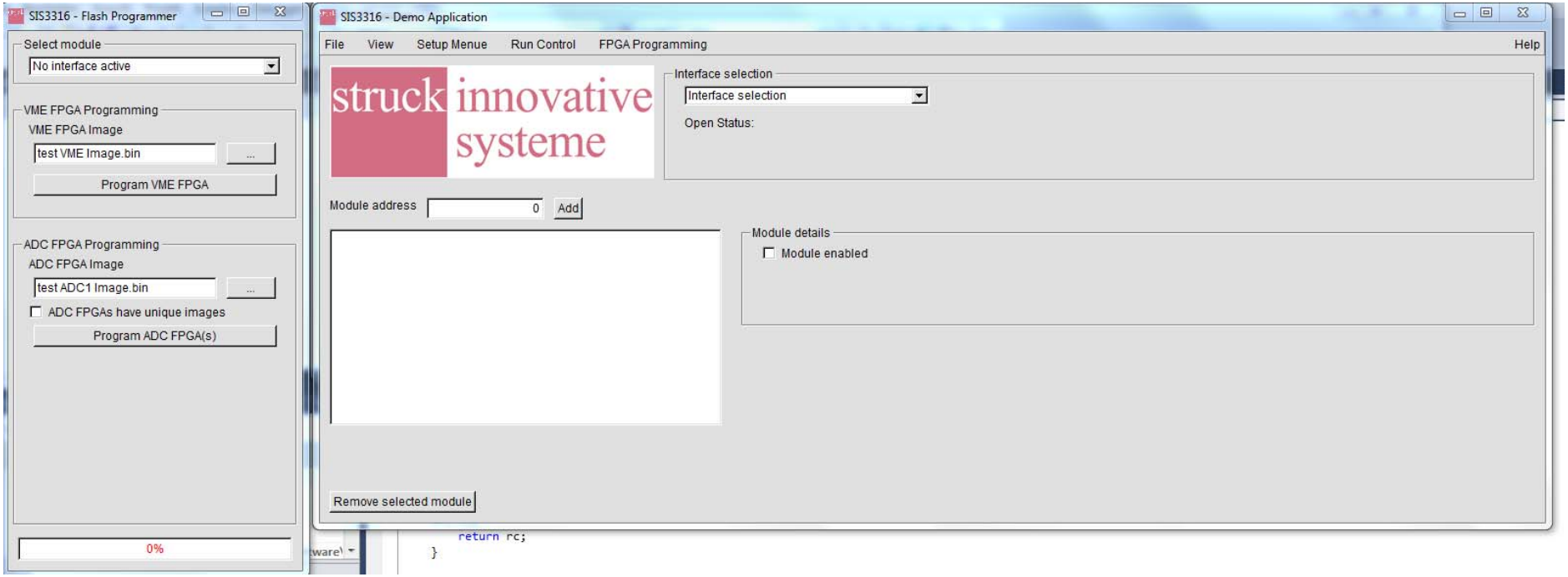
n/Gamma Firmware w. TOF Histogramming



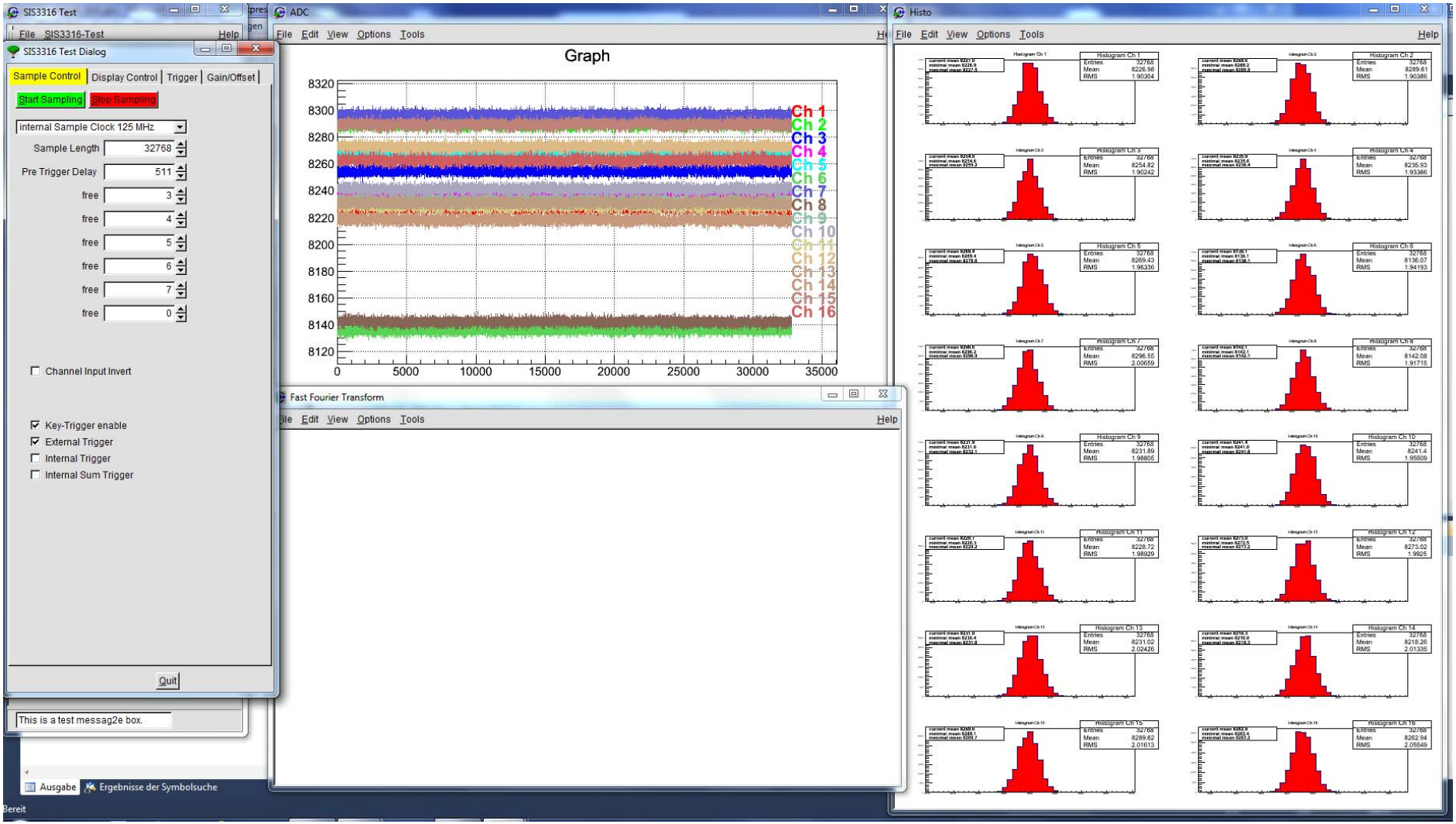
Upcoming Firmware Extensions

- Optical Link Support (upon request)
- VXS Support (upon request)

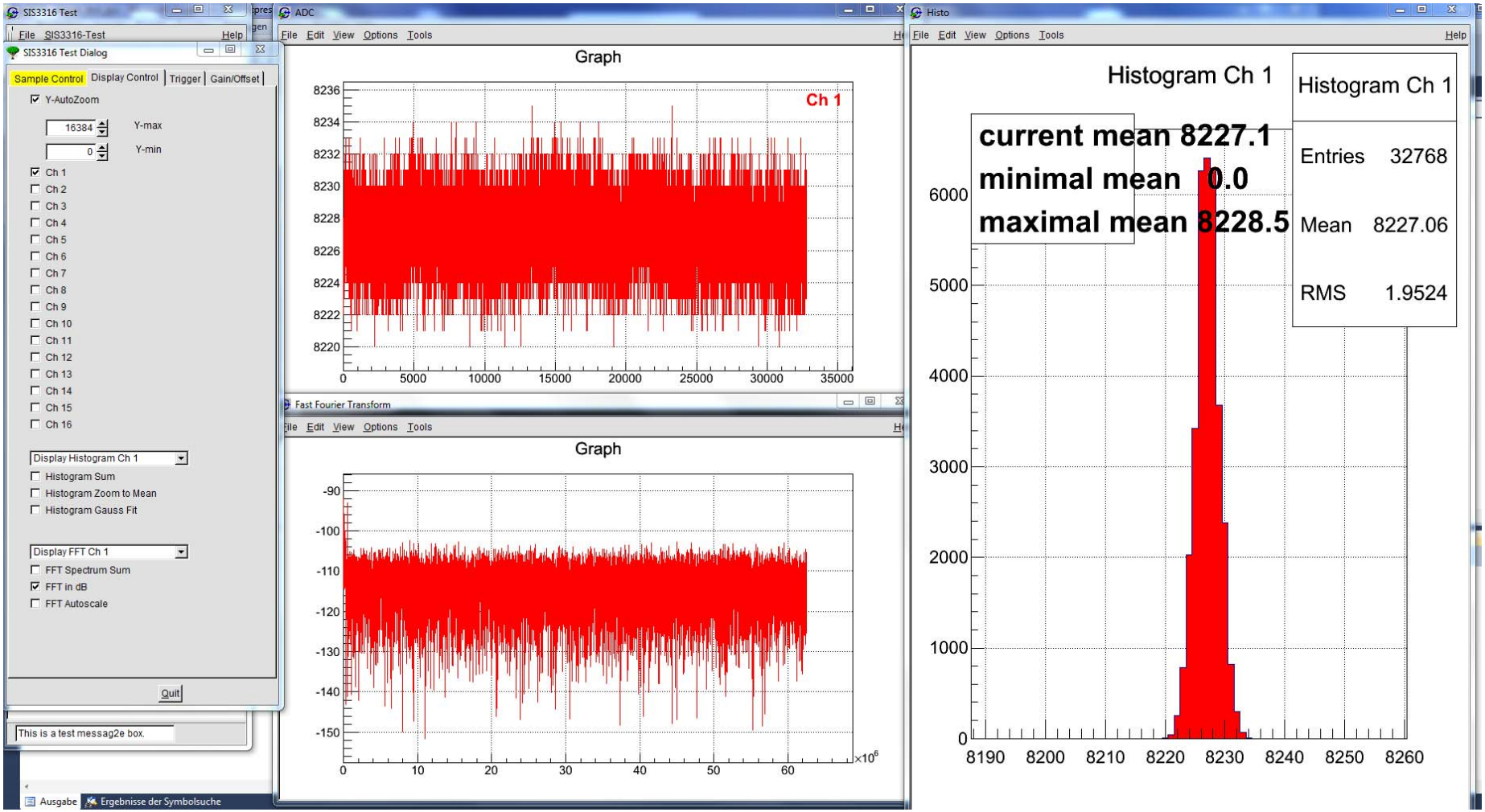
SIS3316 FPGA Flash Programmer (CERN-ROOT based)



SIS3316 Test GUI



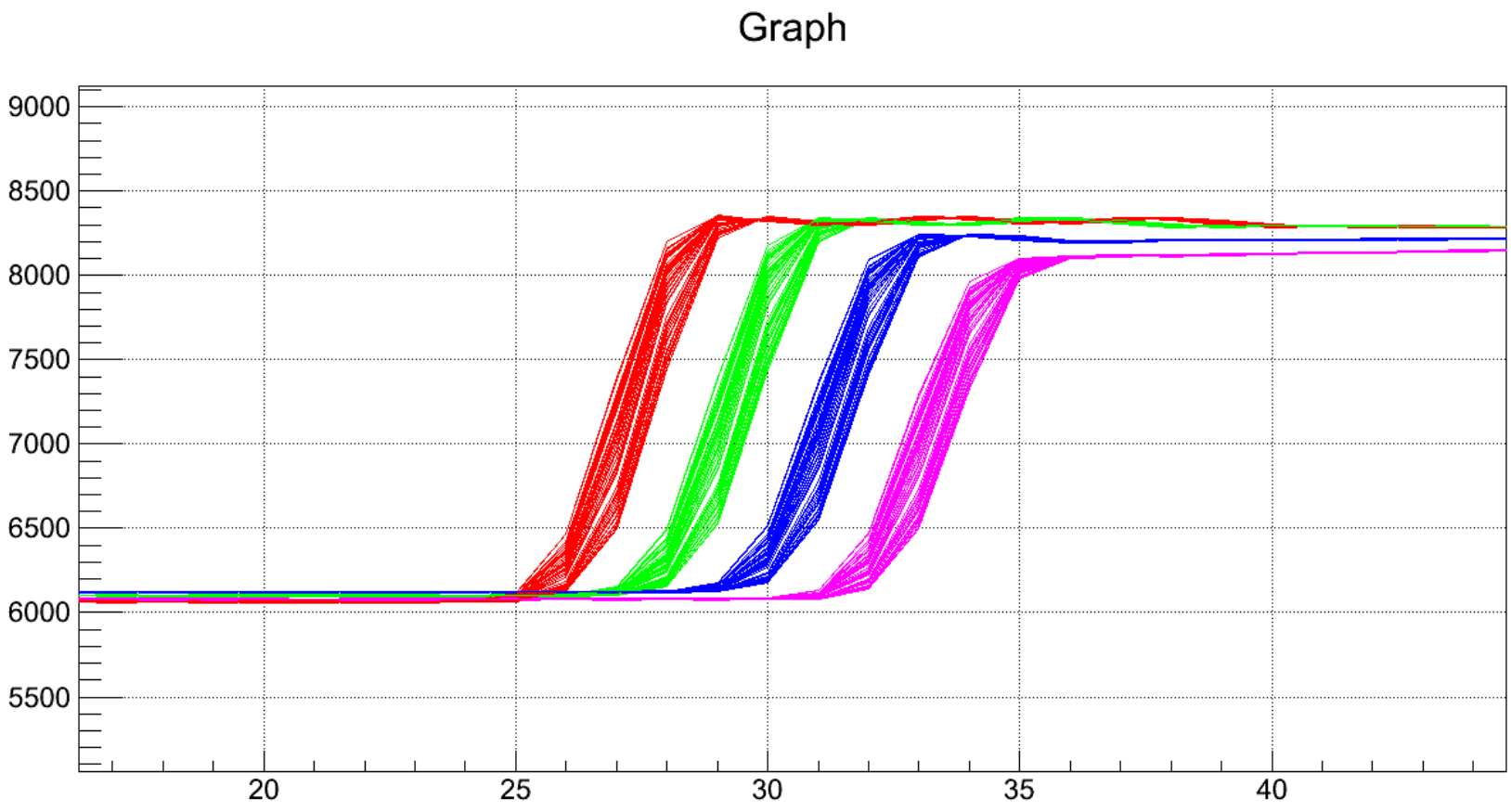
SIS3316 Test GUI



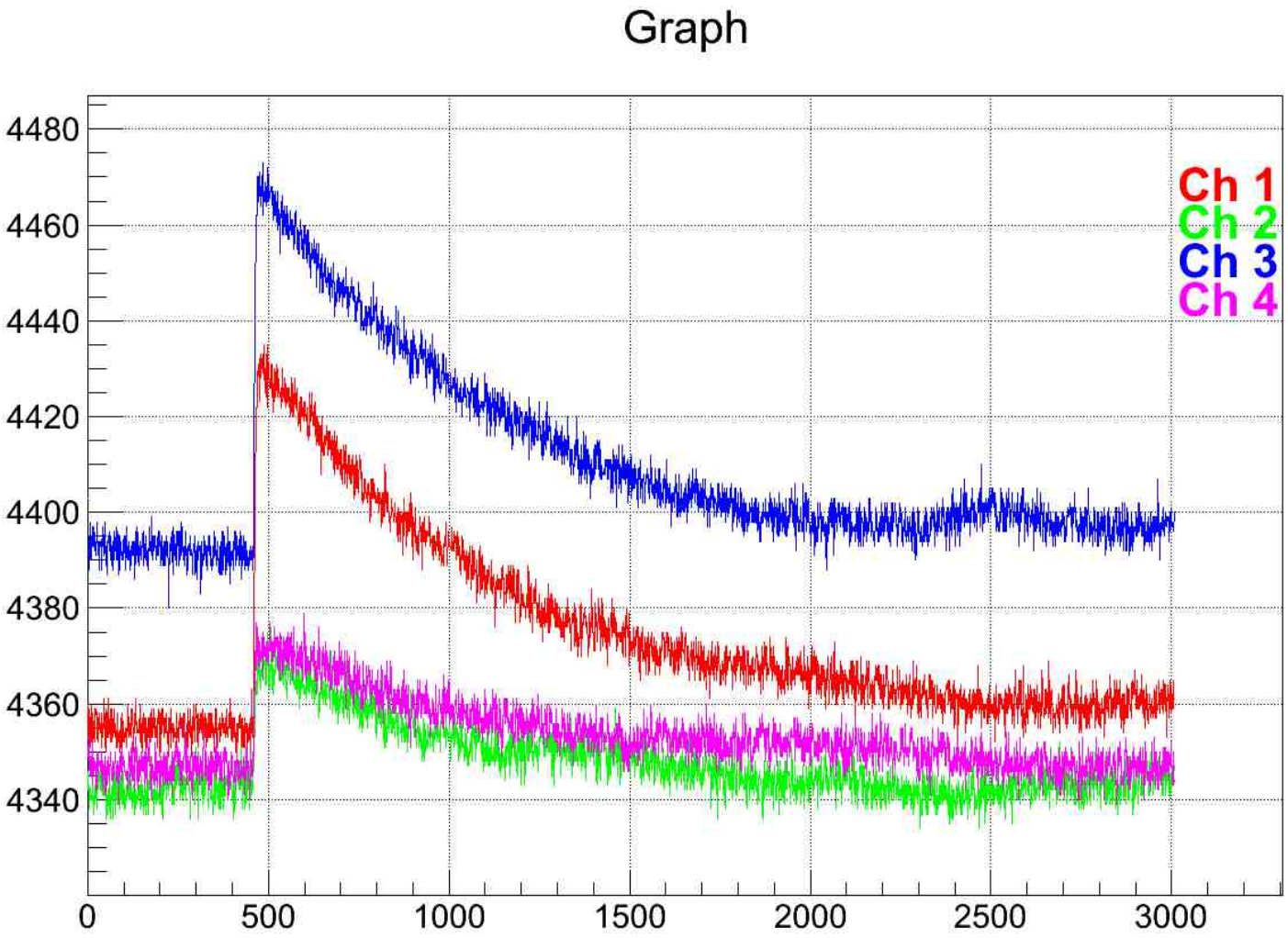
SIS3316 Test Application (CERN-ROOT)

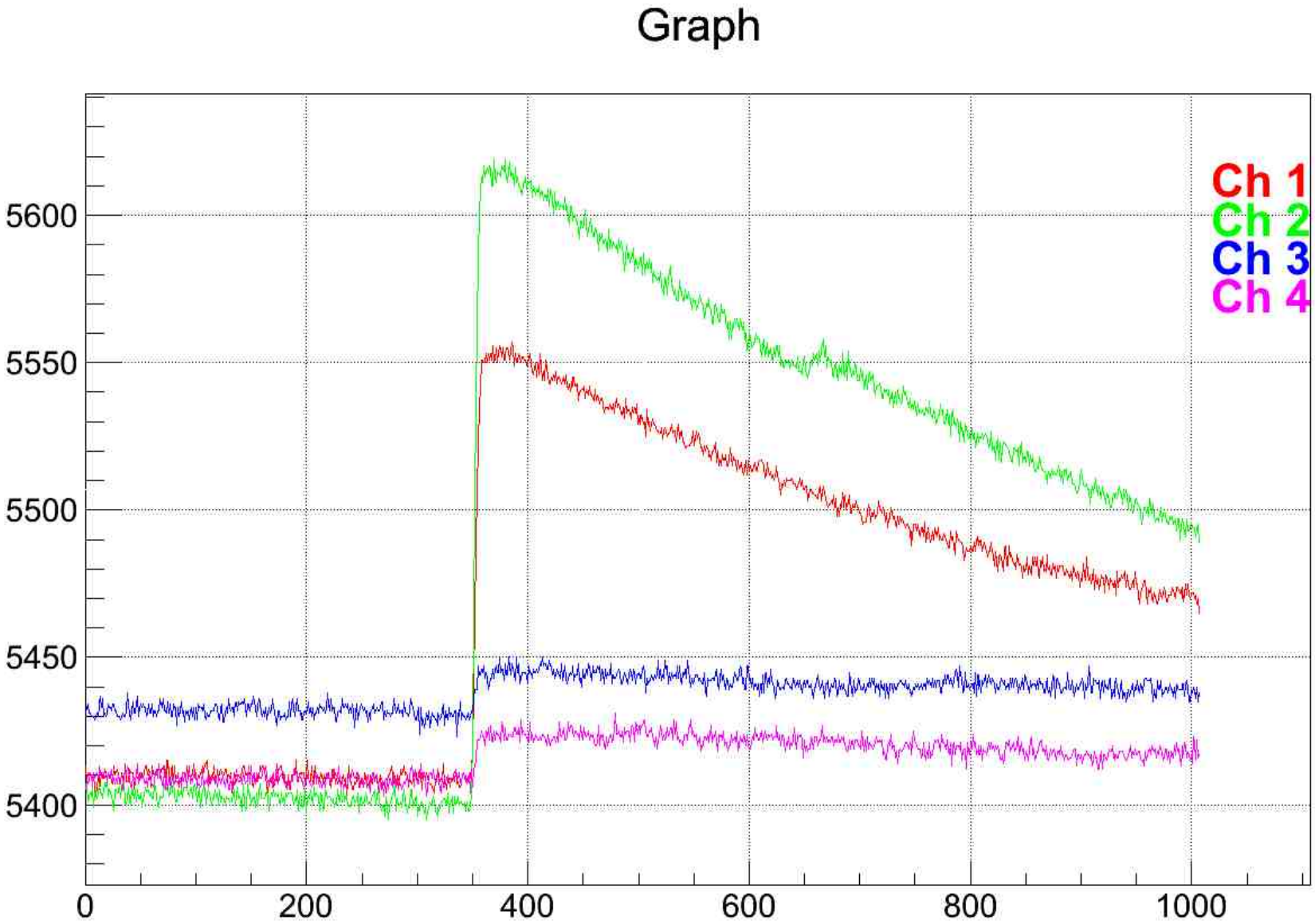
Shows Channel 1 to Channel 4:

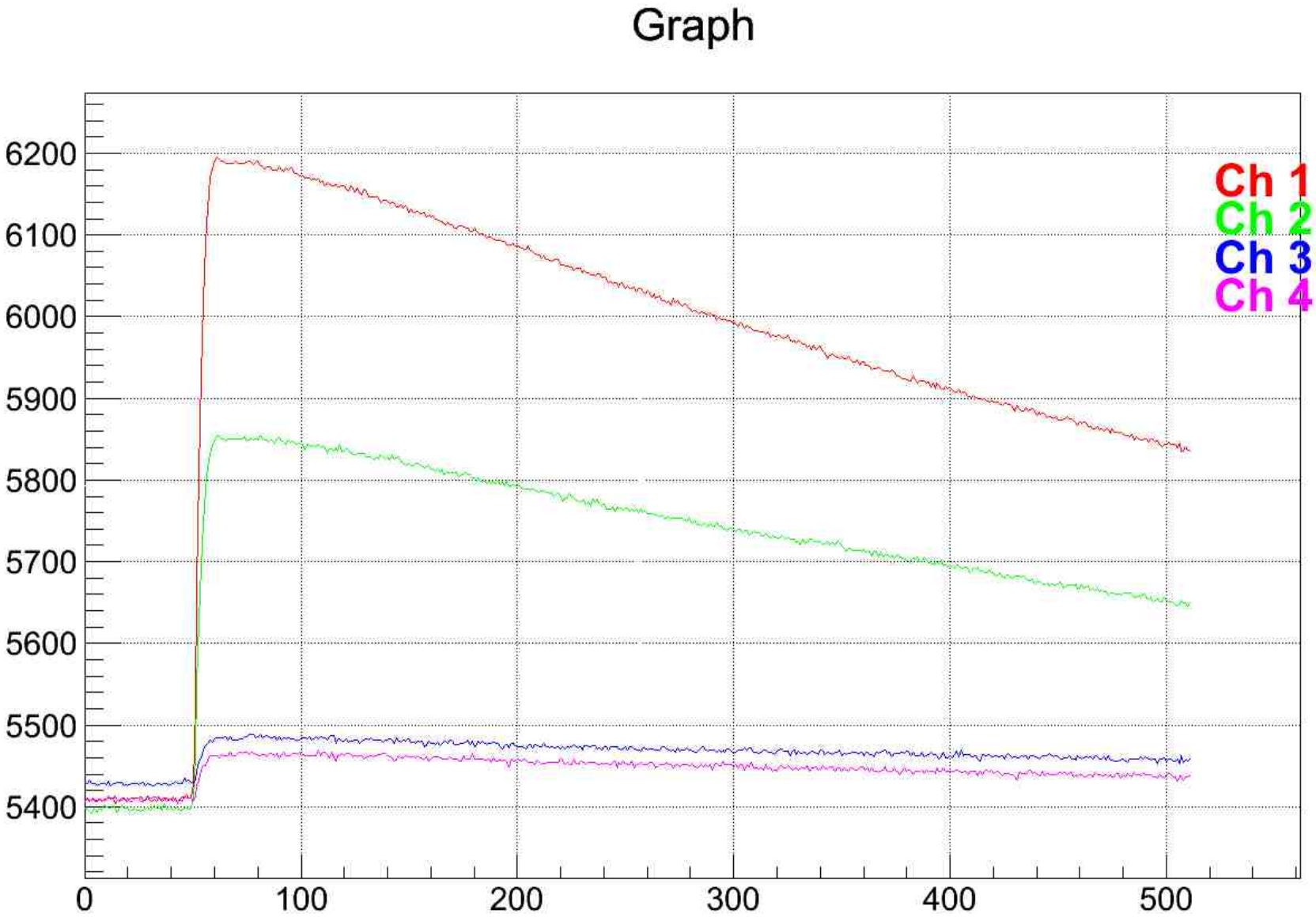
- Signal is delayed with 1.5 meter Lemo cables from ch 1 to ch 2, from ch 2 to ch 3 and from ch 3 to ch 4.



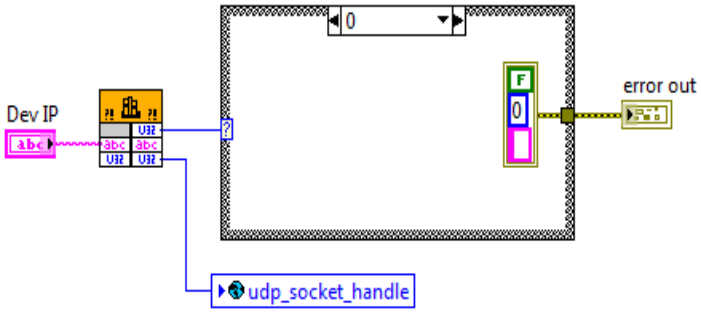
SIS3316 First Measurements at ORNL

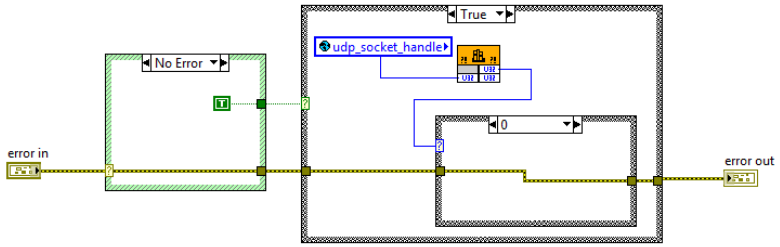


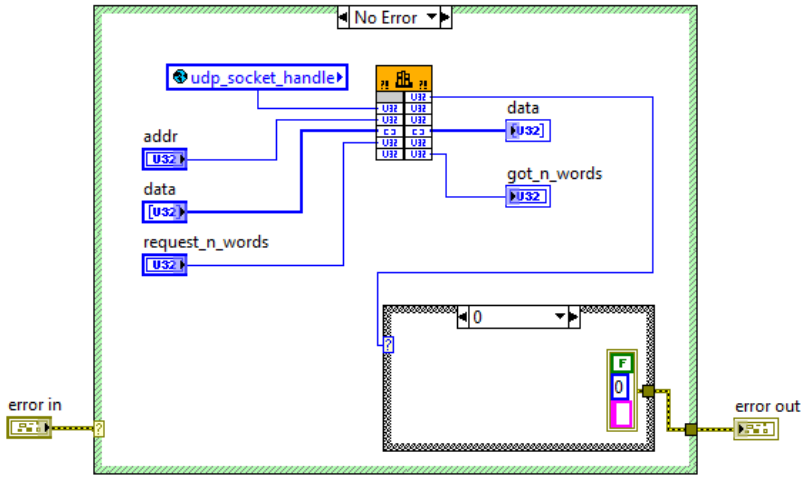

Graph
Ch 1
Ch 2
Ch 3
Ch 4
5600
5550
5500
5450
5400
0
200
400
600
800
1000

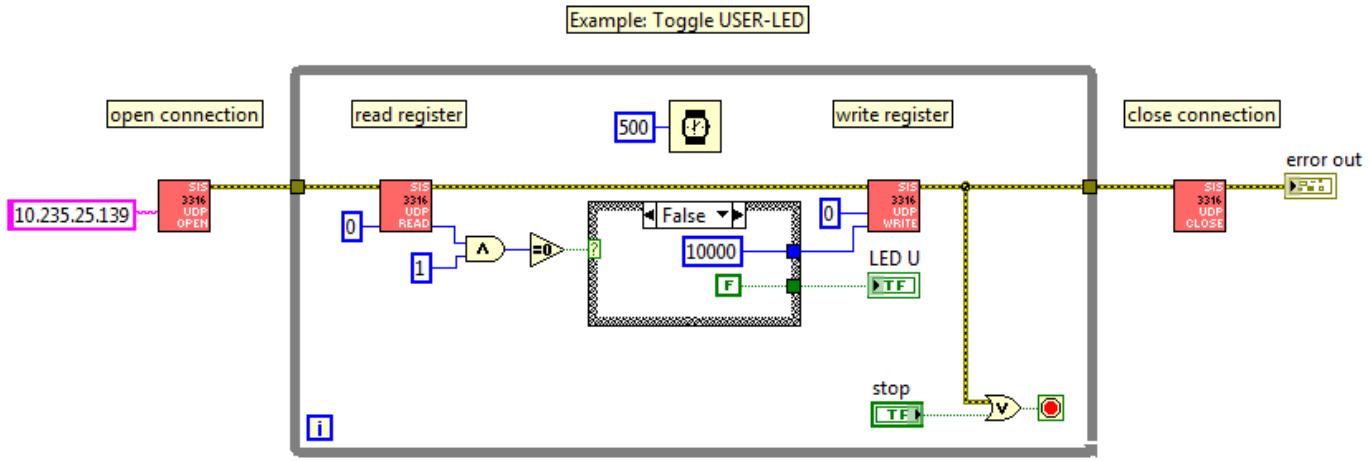

Graph
6200
6100
6000
5900
5800
5700
5600
5500
5400
0
100
200
300
400
500
Ch 1
Ch 2
Ch 3
Ch 4

SIS3316-DT Ethernet Labview Interface

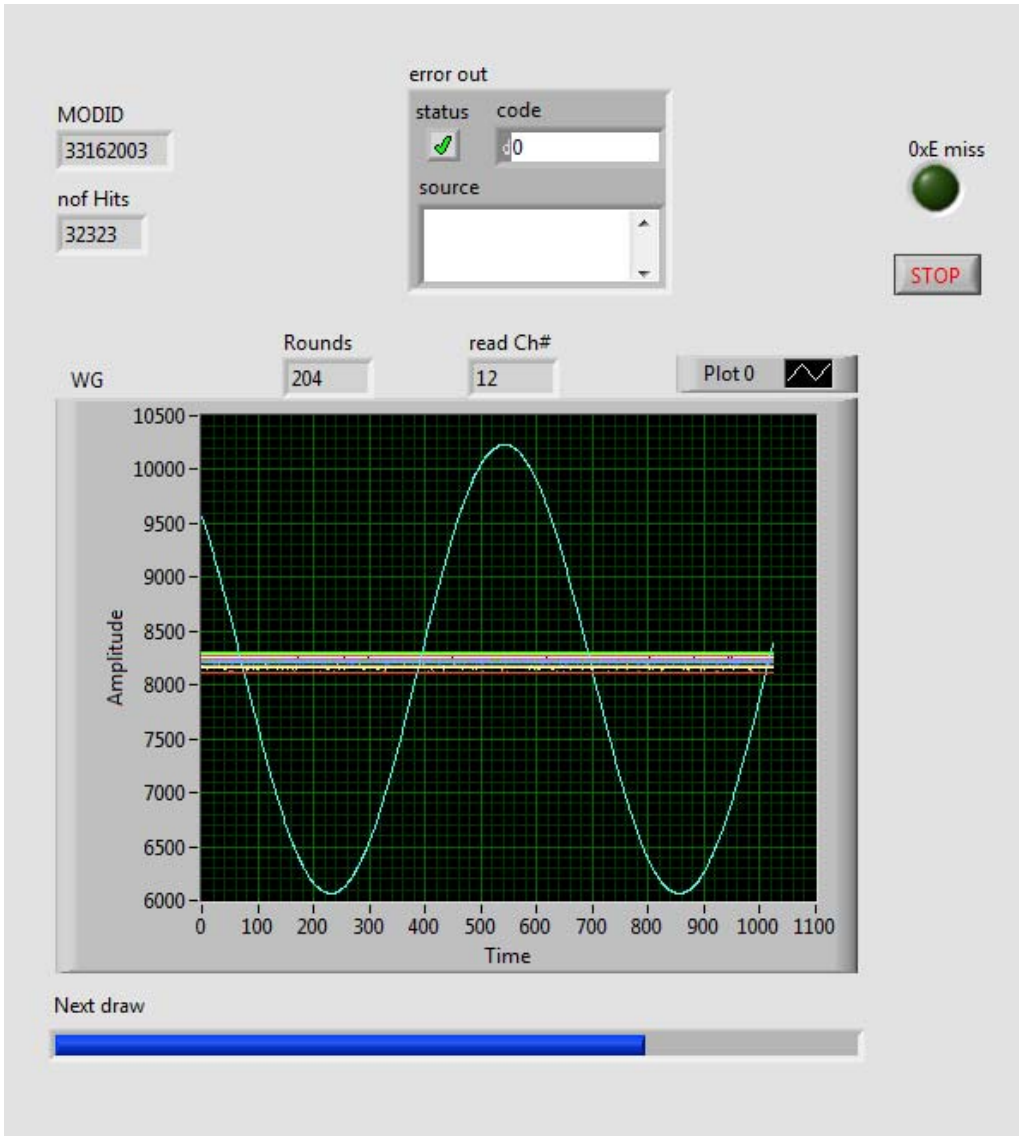


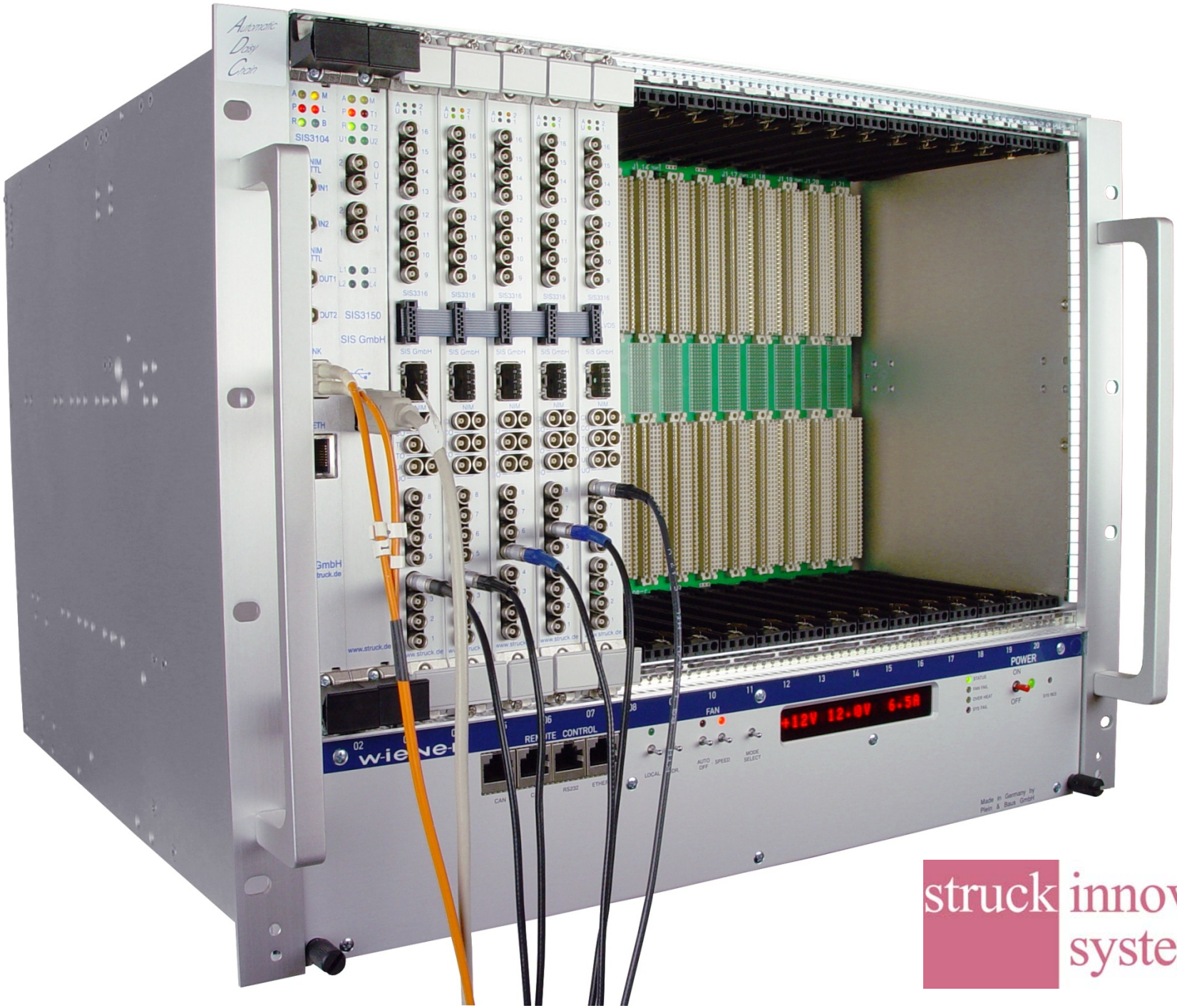






SIS3316-DT Ethernet Labview Interface





struck innovative systeme