White Paper

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MOS Device Aging Analysis with HSPICE and CustomSim

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Abstract

In MOS integrated circuits, device aging is mainly due to the degradation of the gate dielectric and of the interface between gate dielectric and silicon over time. Two important mechanisms that contribute to such degradation are the Hot Carrier Injection (HCI) and the Bias Temperature Instability (BTI). These mechanisms are more prominent in advanced process nodes in which the gate oxide is scaled to only a few molecules in equivalent thickness, and with the use of high-K metal-gate transistors. Long and expensive testing is required to assess the degradation of circuit performance and failure in time (aging), thus increasing the overall manufacturing cost. Alternatively, designers use conservative rules to overdesign the critical circuits, increasing the chip cost. Therefore, a cost-effective way to estimate the lifetime of circuits, especially in mission-critical applications (e.g., automotive electronics), is essential.

MOS Reliability Analysis (MOSRA) in HSPICE® and CustomSim offers a robust and economic alternative to empirical overdesign and extensive lifetime testing. With either the built-in model or user-specified aging model, MOSRA accurately predicts the HCI and BTI aging effect on circuit performance. MOSRA enables designers to detect reliability failures early in the design process, significantly reducing the time and cost of lifetime testing. With tight integration with HSPICE and CustomSim, the aging analysis can be performed as fast as the typical transient simulation runs.

Introduction

The degradation of MOS device characteristics because of aging has become a critical reliability metric for 45nm and below. It degrades circuit performance over time, shortens circuit lifetime and introduces potential failures in the field. One major physical mechanism responsible for device aging is the HCI phenomenon. In the presence of high electric fields, carriers are injected from the drain end of the channel into the gate dielectric, changing its electrical properties over time. Other important aging phenomena are the negative bias-temperature instability (NBTI) for p-channel MOSFETs and the positive bias-temperature instability (PBTI) for n-channel MOSFETs. PBTI is notably present in high-k metal-gate stacks. In both BTI cases, the amount of charges in the gate dielectric changes with the gate bias, because of charge trapping and de-trapping. In the case of a constant bias, the trapped charge will continue to increase, further increasing the threshold voltage (V_{TH}) and decreasing channel carrier mobility. This effect is strongly proportional to the device operating (biasing) temperature. In the situation where the gate voltage is time-varying, some of the trapped charges can even be de-trapped, depending on the trap location and trapping/de-trapping time constants, which leads to a partial recovery of the degradation that has taken place.

MOSRA in HSPICE and CustomSim has been used successfully to identify and debug reliability issues in design at 45nm and below. It delivers:

- Accurate and scalable models for both HCI and BTI, in particular, modeling the partial recovery effect that is essential for BTI
- Seamless integration with the powerful simulation engines in HSPICE and CustomSim to perform electrical stress computation under specified operating conditions and to carry out the stress and degradation over designated operation time period
- Easy integration of custom models developed by device modeling teams in foundries and/or design houses
- Accounting for the stress accumulation effect, which refers to, for example, the fact that as a MOS device is aged, the drain current decreases, and that, in turn, slows down the subsequent device degradation.

MOSRA Aging Models

Device aging is a result of continuous degradation of device characteristics, under the applied electrical stress. A MOSRA model is used for translating the amount of electrical stress to the actual device degradation, or “age”. Typically, such models are a function of device operating conditions (i.e., voltages, currents, and temperatures) as well as device geometries. The resulted degradation can be applied in two ways:

1. The amount of stress is converted in the degradation of key MOSFET compact model parameters (e.g., threshold voltage, mobility, etc.)
2. As an alternative, the stress can be directly converted into a degradation of device characteristics (e.g., direct percentage degradation of the drain current and of its conductance).

While the second approach has the advantage of simplicity, the first approach allows for a separation of different effects that contribute to the total device degradation, resulting in better accuracy of current and conductance degradation over a wide range of device biases.

MOSRA models are constructed with physics-based formulations and augmented with coefficient parameters to improve the model accuracy and parameter extraction flexibility.

MOSRA BTI models

For N/PBTI models, two principal physical mechanisms are considered: One related to the contribution of the interface traps (Equation 1) and the other related to the traps deep inside the dielectric layer (Equation 2).

$$\Delta V_{TH,IT} \sim \exp\left(-\frac{E_a}{K \cdot T}\right) \cdot \left[\frac{\varepsilon}{t_{ox}}(V_{gs} - V_{TH})\right]^{TITCE} \cdot \exp\left[TITFD \cdot E\left(V_{gs}, V_{ds}\right)\right] \cdot t^{NIT} \qquad \textbf{(1)}$$

$$\Delta V_{TH,OT} \sim \exp\left[-\frac{TOTFD + \frac{TOTTD}{T}}{E\left(V_{gs}, V_{ds}\right)}\right] \cdot t^{NOT} \qquad \textbf{(2)}$$

In the above equations, $E(V_{GS}, V_{DS})$ denotes the strength of the electric field of the dielectrics. The degradation of the device threshold voltage is employed for the illustration of the BTI models.

Recent submicron device data shows a significant dependence of NBTI and PBTI on the channel length. The dependence trend varies based on process conditions. According to these observations, we have included flexible channel width- and length-dependence equations. While our BTI modeling solution allows a binning approach, the geometry scaling equations embedded in the model provide for accurate global modeling.

The partial-recovery effect (Figure 1) is modeled by taking into account the stress stimulus duty cycle. When the partial-recovery effect is considered, the total degradation becomes smaller:

$$\Delta V_{TH,AC} = TTD0 \cdot \Delta V_{TH} \cdot \exp(-TDCD \cdot g) \qquad \textbf{(3)}$$

where the g quantity models the effect of duty cycle.

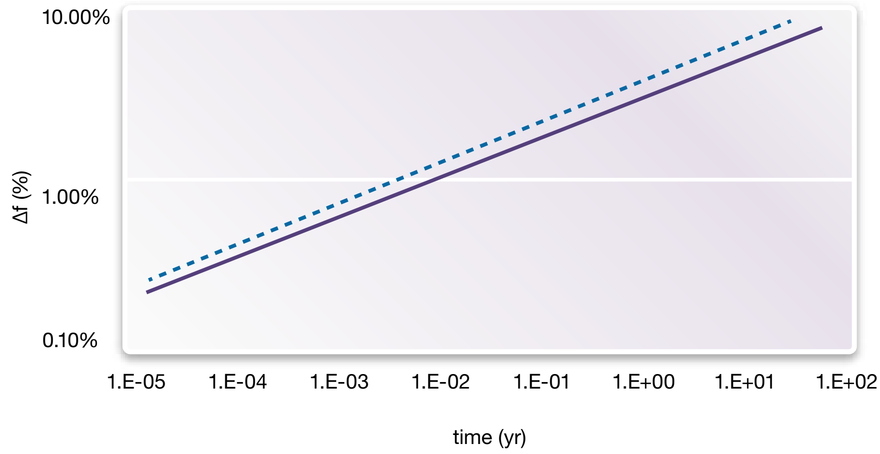

Figure 1: The effect of partial recovery on the ring oscillator frequency degradation. The dashed line represents the degradation without partial recovery

This approach to modeling the BTI partial recovery allows us to consider its effect on degradation dynamically, as a function of circuit operating time (see Figure 2).

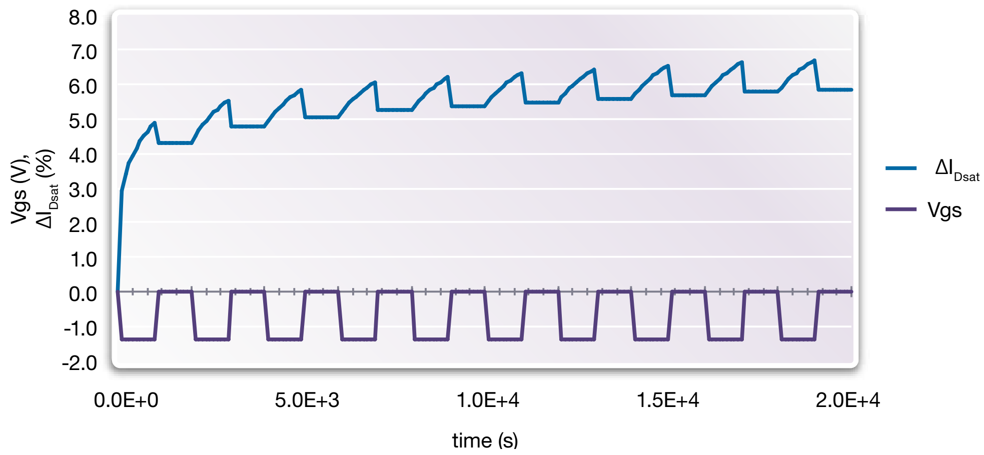

Figure 2: Partial recovery of degradation during circuit operation, as illustrated based on device I_{Dsat} degradation

MOSRA HCI models

The HCI model should accurately account for bias dependence over a wide range of drain, gate and substrate biases, and over different temperatures. This accuracy should be maintained over a wide array of channel lengths and for different oxide thicknesses. The basic formulation of the MOSRA HCI model is as follows:

$$\Delta V_{TH,HCI} \sim THCI1 \cdot \left(\frac{I_{ds}}{W_{eff}}\right)^{TDCE} \cdot \left(\frac{I_{sub}}{I_{ds}}\right)^{TDII} + THCI2 \cdot V_{ds}^{TDVD} \cdot \left(\frac{I_{ds}}{W_{eff}}\right)^{TDID} \quad \textbf{(4)}$$

where the first term corresponds to the Lucky Electron Model [1], and the second term improves model accuracy in the high current regime.

A dedicated and more accurate MOSFET impact ionization current model is included in the MOSRA HCI model. This can be used as an alternative to the substrate current from existing compact models, such as BSIM4 (see Figure 3).

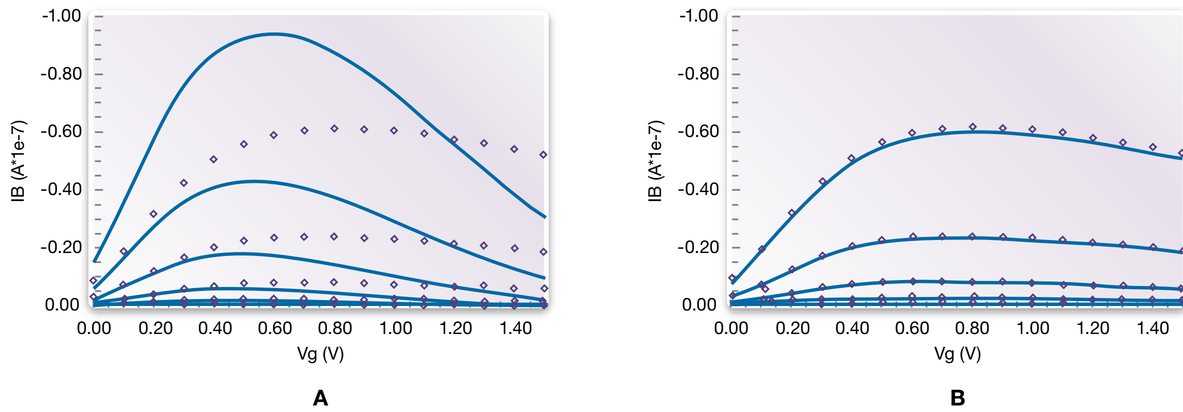

Figure 3: The I_{SUB} model of BSIM4 model (A) vs. the HCI impact ionization current model (B). The lines represent the simulated curves, the dots represent the data points.

MOSRA Flow

MOSRA capability is implemented in HSPICE and CustomSim. The MOSRA flow includes two phases: the pre-stress simulation phase and the post-stress simulation phase, respectively (see Figure 3). The two simulation phases can be executed either in the same simulator run, or independently, as needed.

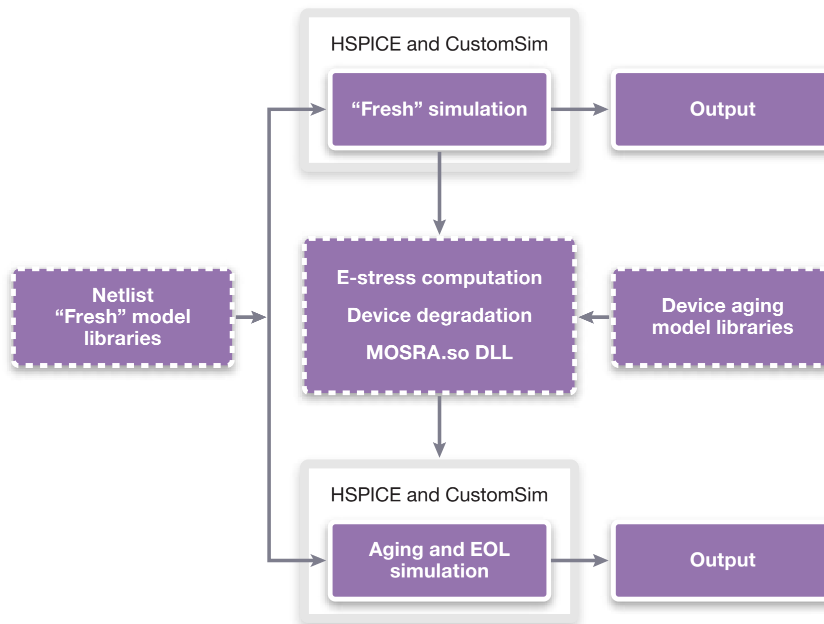

Figure 4: The MOSRA Flow

In Figure 4, EOL refers to the end of lifetime of a MOS device, defined as the device operation time at which the device parameters such as IDsat degrades by a given percentage (typically, 10%) of its fresh (un-aged) value.

Pre-stress simulation

During the pre-stress ("fresh") simulation phase, the simulator computes the electrical stress of user-selected MOSFETs in the circuit, based on the MOSRA models. The calculation depends on the electrical simulation conditions of each targeted device. The stress value from the MOSRA equation is integrated over a user-specified simulation time interval, through the duration of the transient analysis.

The result of the integration is then extrapolated to calculate the total stress after a user-specified time of circuit operation (age).

Post-stress simulation

During the post-stress phase, a second simulation is launched. The degradation of device characteristics is therefore translated to performance degradation at the circuit level. The post-stress MOSRA simulation phase can be based on either .DC, .AC or on .TRAN analysis.

The effect of accumulated stress illustrates the aging simulation capabilities due to a seamless integration of the aging models within the MOSRA flow. At each MOSRA circuit operation time step the flow considers the accumulated degradation information from previous time steps. As a result, the accumulated stress effect is taken into account implicitly, with no need for empirical "equation bending" (see Figure 5).

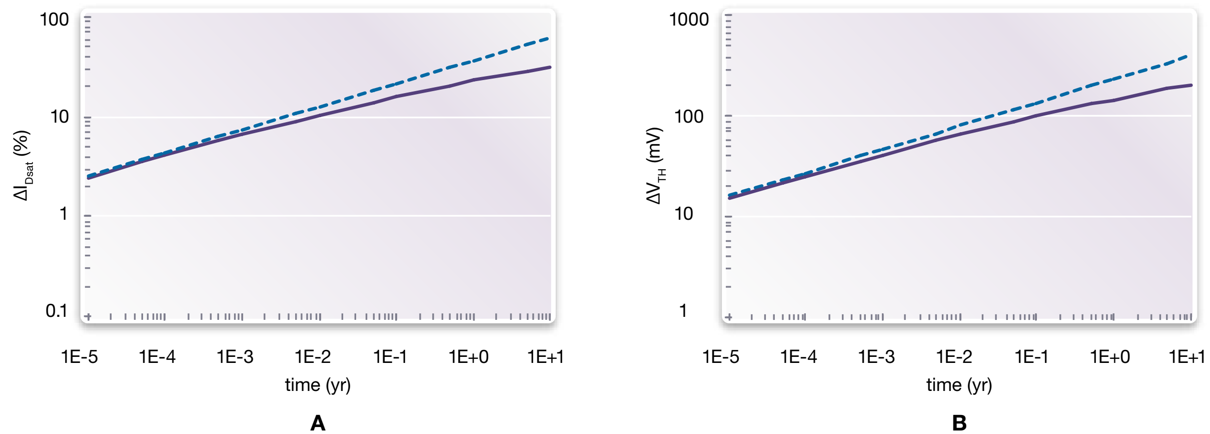

Figure 5: The effect of accumulated stress on I_{Dsat} (A) and on V_{TH} (B). The dashed line represents the degradation without the effect of accumulated stress, which produces unnecessarily pessimistic circuit lifetime

User-defined HCI and BTI modeling

In addition to the proprietary HCI and BTI models discussed in section 2, HSPICE AND CustomSim enable foundries and IDMs to develop their own HCI and BTI models then integrate them with the simulator through an API. Users can implement and compile their own special model equations through the API, and compile them into a Dynamically Linked Library (DLL).

Summary

MOS Reliability Analysis (MOSRA) in HSPICE and CustomSim offers an accurate and efficient solution for analyzing the degradation of integrated circuit performance over time as a result of MOS device aging. The solution accurately models the HCI and BTI aging mechanisms and analyzes their impact on circuit performance using actual circuit operation and stimulus. MOSRA comes with a built-in aging model that is silicon-proven down to 28nm. It also gives modeling teams the flexibility to integrate their in-house models. MOSRA is tightly integrated with the powerful engines in HSPICE and CustomSim, running post-stress analysis as fast as pre-stress runs.

References

[1] C.Hu et al., "Hot-electron-induced MOSFET degradation — Model, monitor, and improvement", IEEE Journal of Solid-State Circuits, vol. SC-20, no. 1, pp. 295-305 (1985).

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