*Technical White Paper*

# *Demystifying LDO Turn-On (startup) Time*

*Stephen Ziel*

**ABSTRACT**

This paper provides a comprehensive discussion on what affects the total turn on time in modern LDO regulators. It describes a new mathematical foundation to calculate the turn-on ramp time for many modern LDO regulators which employ either a noise reduction (NR) filter, feedforward (FF) capacitor ($C_{FF}$) or both. The designer can use this new analysis set to perform statistical calculations on LDO regulator turn-on time. This analysis helps assess the device minimum and maximum turn-on times and also the expected inrush current. Designs which must meet a maximum slew rate requirement during turn on (or *rate-of-rise* requirement) can also use this new analysis set to confirm that an startup ramp rate meets the system requirements.

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## Trademarks

# 1 Introduction to linear regulator turn-on time

The turn-on time ($t_{ON}$) for an LDO regulator is a summation of the delay time ($t_D$) and the rise time ($t_R$) (see Equation 1 and Figure 1-1). The delay time is defined as the fixed time delay from when the output voltage can start to increase with respect to an external stimulus, to when the output voltage actually begins to increase. If the LDO regulator has an enable pin, the external stimulus typically occurs when the enable voltage toggles to turn on the LDO regulator. This behavior assumes that the input voltage has already been applied to the input of the LDO regulator. For LDO regulators without an EN pin, the input voltage acts as the external stimulus.

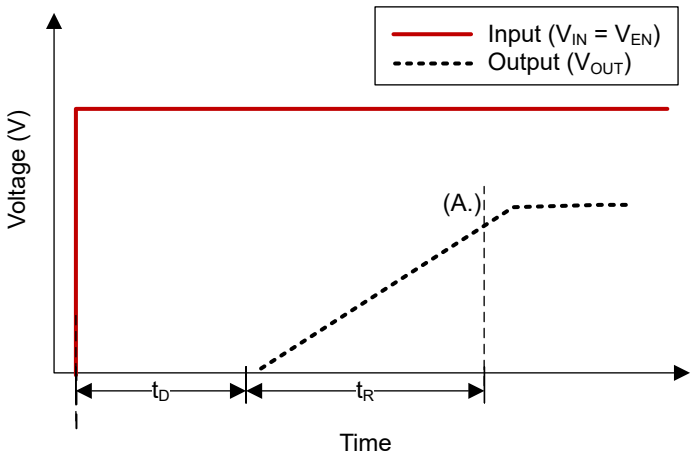



**Figure 1-1. Total turn-on time vs input voltage**

A. Minimum $V_{OUT}$ regulation

$$t_{ON} = t_D + t_R \quad (1)$$

Delay time for an LDO regulator is usually small compared to the rise time. Delay times result from how quickly the device can energize internal circuitry to begin increasing the output voltage. The LDO regulator data sheet gives the best estimate of the delay time because after the device is enabled, external circuitry has little influence on the delay time. The rise time is the time to increase the output voltage from 0V to the minimum regulation. Each application requires unique regulation so the minimum regulation point is application specific. For example, one design may allow a tolerance of ± 3% while another design may allow a tolerance of ± 5%. Thus, the turn-on time is faster for a design with wider tolerance requirements.

# 2 What impacts the LDO rise time?

Linear regulator references can use either a precision voltage source (Figure 2-1) or a precision current source (Figure 2-2). The linear regulator turn-on time is affected by either the reference turning on or the RC time constant formed by the $R_{TOP}$ and $C_{FF}$ in the feedback loop. Typically, the reference voltage turns on very quickly, however in modern LDO regulators the reference voltage may also be filtered through a low pass noise reduction (NR) resistor and capacitor.

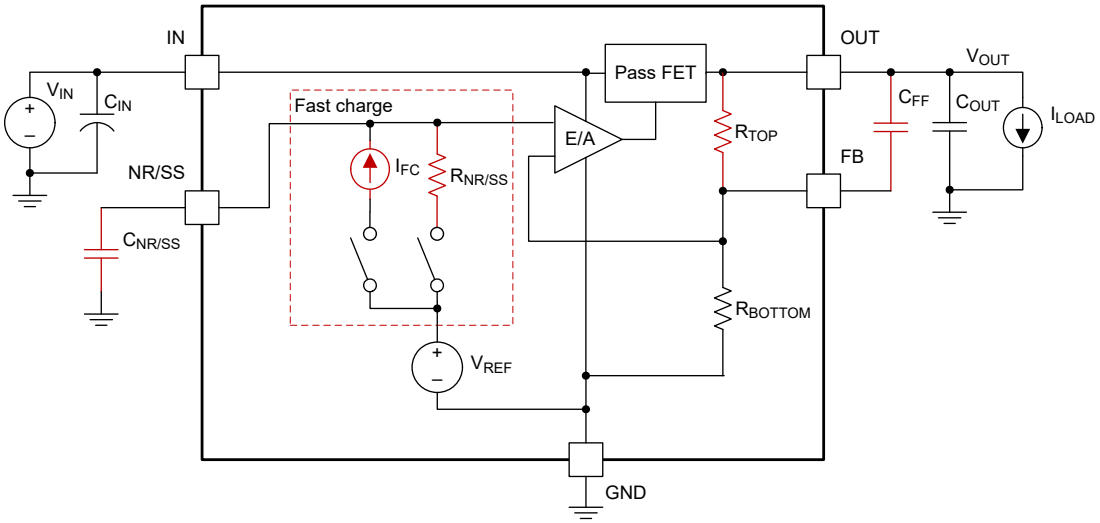



**Figure 2-1. Precision voltage reference**

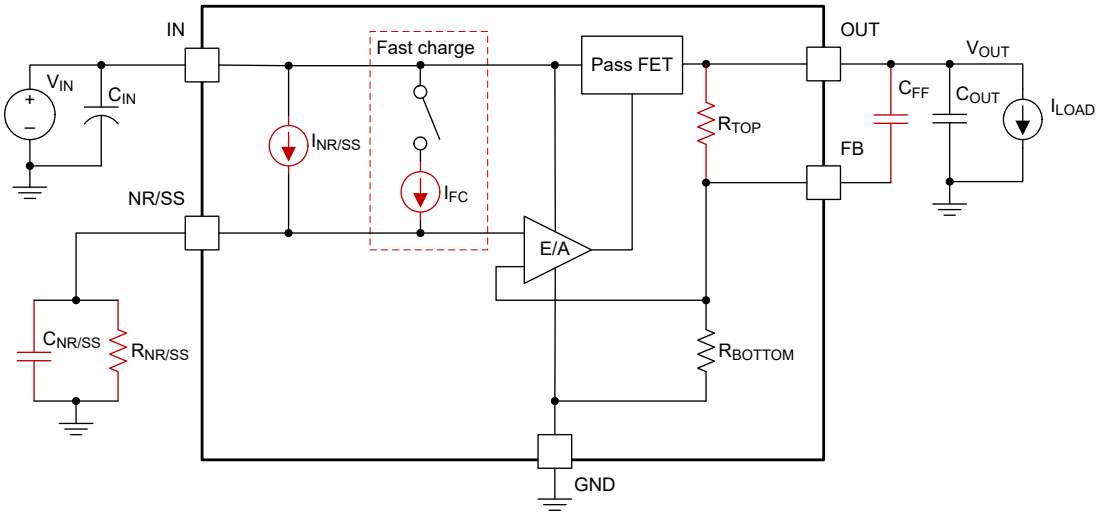



**Figure 2-2. Precision current reference**

Voltage across the $R_{TOP}$ resistor ramps in accordance with both the RC time constants on $V_{REF}$ and $R_{TOP}$. Equation 2 represents the NR/SS time constant and Equation 3 represents the FF time constant.

$$\tau_{NR/SS} = R_{NR/SS} \times C_{NR/SS} \quad (2)$$

$$\tau_{FF} = R_{TOP} \times C_{FF} \quad (3)$$

During the turn-on period, the voltage on the VOUT pin is the summation of the voltage across the $R_{BOTTOM}$ resistor (or $V_{FB}$) and the voltage across the $R_{TOP}$ resistor (or $V_{TOP}$) as shown in Equation 4 :

$$V_{OUT}(t) = V_{TOP}(t) + V_{FB}(t) \quad (4)$$

During the turn-on period, the reference voltage ramps fast enough for it to approximate an ideal step function relative to the much longer $\tau_{NR/SS}$ time constant. Equation 5 describes $V_{FB}(t)$ when the LDO regulator reference is a precision voltage source, but when it is a precision current source, use Equation 6 instead.

$$V_{FB}(t) = V_{REF} \times \left(1 - e^{-\frac{t}{\tau_{NR/SS}}}\right) \quad (5)$$

$$V_{FB}(t) = I_{NR/SS} \times R_{NR/SS} \times \left(1 - e^{-\frac{t}{\tau_{NR/SS}}}\right) \quad (6)$$

The voltage across the top set point resistor is more complex to calculate as $V_{FB}(t)$ is not always a step function. When $\tau_{NR/SS}$ and $\tau_{FF}$ are comparable values, neither time constant dominates the turn-on calculation. Use Laplace transforms and partial fraction expansions [1]-[2] to derive $V_{TOP}(t)$, shown in Equation 7.

$$V_{TOP}(t) = V_{REF} \times \frac{R_{TOP}}{R_{BOTTOM}} \times \left(1 - \frac{\tau_{NR/SS}}{\tau_{NR/SS} - \tau_{FF}} \times e^{-t/\tau_{NR/SS}} - \frac{\tau_{FF}}{\tau_{FF} - \tau_{NR/SS}} \times e^{-t/\tau_{FF}}\right) \quad (7)$$

## 2.1 Simple Use Cases

When $\tau_{NR} \gg \tau_{FF}$, or when the LDO regulator operates in unity gain feedback (when $R_{TOP}$ = 0Ω), the turn-on time is dominated by $\tau_{NR}$ and Equation 8 represents $V_{OUT}(t)$.

$$V_{OUT}(t) \cong V_{FB}(t) \times \left(\frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}}\right) \quad (8)$$

When $\tau_{NR} \ll \tau_{FF}$, Equation 7 can be simplified to Equation 9 :

$$V_{TOP}(t) \cong V_{REF} \times \frac{R_{TOP}}{R_{BOTTOM}} \times \left(1 - e^{-t/\tau_{FF}}\right) \quad (9)$$

### *2.1.1 Case 1: LDO with an NR filter but without $C_{FF}$ capacitance*

Figure 2-3 shows the TPS7A20 [3]. The analysis uses Equation 5 and Equation 8 to calculate the turn-on time.

Equation 10 calculates the tau of an RC circuit using the 10% to 90% time measurement ($t_{10\%-90\%}$). Use Equation 5, Equation 8, and Equation 10 to calculate $t_R$ for any regulation band requirement in Figure 1-1. The measured turn-on time for Figure 2-3 is 258.7µs which equates to $\tau$ = 117µs for the TPS7A20.

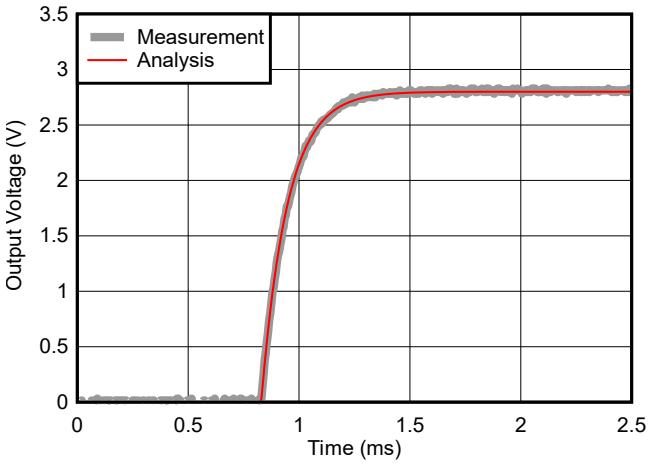



**Figure 2-3. TPS7A20 turn-on timing**

$$\tau_{RC} = \frac{t_{10\% - 90\%}}{\ln 9} \quad (10)$$

### *2.1.2 Case 2: NR filter with a $C_{FF}$ capacitance*

Figure 2-4 shows the TPS7A49 turn-on analysis versus the physical measurement. The analysis uses Equation 4, Equation 5, and Equation 7 to calculate the turn on time. $R_{TOP}$ = 11.5kΩ, $R_{BOTTOM}$ = 1.02kΩ and $C_{FF}$ = 100nF.

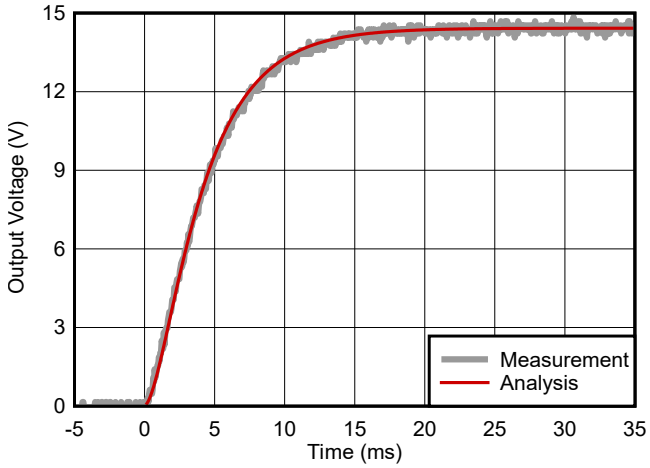



**Figure 2-4. Output voltage vs Time**

### *2.1.3 Fast-charge circuitry*

The NR/SS filter significantly improves the power supply rejection ratio (PSRR) and noise in LDO regulators. [21]

The time constant for the NR/SS filter may result in longer than desired turn-on times for some applications. Modern LDO regulators may include a *fast charge* circuit to reduce the turn-on time of the filtered reference supply, and by extension, the output voltage. The fast-charge circuit operates while $V_{NR/SS}$ measures less than the changeover voltage ($V_{CO}$), when the steady state filter values are used.

Figure 2-5 shows typical turn-on behavior of an LDO regulator using fast charge.

For LDO regulators that use a voltage reference, this fast-charge circuit is either a parallel current source or parallel resistor with the NR/SS resistor as shown in Figure 2-1. For LDO regulators that use a current reference, the fast-charge circuit modifies the $I_{REF}$ current to be a larger value as shown in Figure 2-2. Equation 11 calculates the time when the changeover voltage occurs ($t_{CO}$). Entering $\tau = t_{CO}$ into Equation 7 yields the initial condition ($V_{CO\_FF}$) on $V_{TOP}$ just after the changeover voltage event.

If a fast-charge current source is across $R_{NR/SS}$, use Equation 12 instead of Equation 11 to calculate $t_{CO}$.

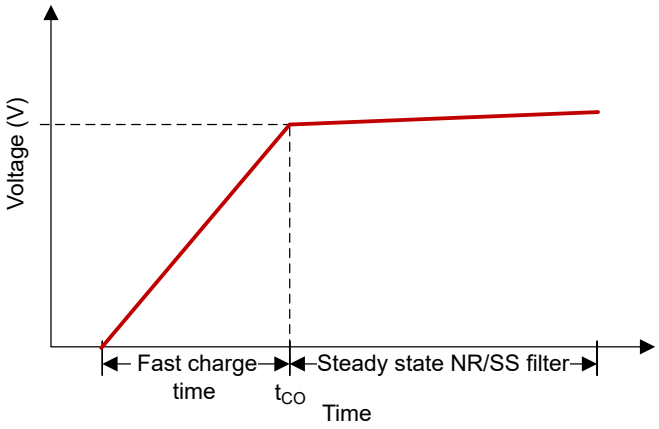



**Figure 2-5. Changeover voltage vs time**

$$t_{CO} = -\tau_{NR/SS} \times \ln\left(1 - \frac{V_{CO}}{V_{REF}}\right) \quad (11)$$

$$t_{CO} = -\tau_{NR/SS} \times \ln\left(1 - \frac{V_{CO}}{V_{REF} + I_{FC} \times R_{NR/SS}}\right) \quad (12)$$

Common values of $V_{CO}$ are 95% to 97% of $V_{REF}$. Use Equation 5 or Equation 6 to calculate $V_{FB}(t)$ during fast-charge operation, but after the fast-charge function completes, use Equation 13.

$$V_{FB}(t) = V_{REF} + (V_{CO} - V_{REF}) \times \left(e^{-\frac{t - t_{CO}}{\tau_{NR/SS}}}\right) \quad (13)$$

If the LDO uses a precision current source, (as shown in Figure 2-2) use Equation 14.

$$V_{REF} = I_{NR/SS} \times R_{NR/SS} \quad (14)$$

Use Equation 15 to calculate $V_{TOP}$ after the changeover event. Equation 13 defines $V_{FB}(t)$.

$$V_{TOP}(t) = V_{FB}(t) \times \frac{R_{TOP}}{R_{BOTTOM}} + \left(V_{CO\_FF} - V_{FB}(t) \times \frac{R_{TOP}}{R_{BOTTOM}}\right) \times \left(e^{-\frac{t - t_{CO}}{\tau_{FF}}}\right) \quad (15)$$

### *2.1.4 Non-ideal LDO behavior*

The following conditions can affect the total turn-on time of an LDO regulator.

#### 2.1.4.1 Applied voltage bias

In general, applied voltage bias has a minor impact to the turn-on time. Changes to the effective capacitance of modern ceramic capacitors due to voltage bias require significant amounts of time [20]. The typical LDO regulator turn-on times are too short to meaningfully impact $C_{NR/SS}$ and $C_{FF}$ capacitance due to the change in voltage bias. Exceptions to this generalization are rare use cases where the LDO regulator is purposely designed for a long turn-on time while simultaneously operating without current limit engaged.

#### 2.1.4.2 Fast charge current tolerance

The fast charge current source has a tolerance which can impact to the soft-start time if the variation is large. $I_{FC}$ can shift across process tolerances, temperature and different values of $V_{IN}$ or $V_{BIAS}$.

Table 2-1 lists fast-charge current tolerance from the TPS7A91 data sheet.

**Table 2-1. Electrical specifications**

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{NR/SS}$ | NR/SS pin charging current | $V_{NR/SS}$ = GND, $V_{SS\_CTRL}$ = GND | 4.0 | 6.2 | 9.0 | µA |
| | | $V_{NR/SS}$ = GND, $V_{SS\_CTRL}$ = $V_{IN}$ | 65 | 100 | 150 | |

#### 2.1.4.3 Internal error amplifier offset voltage

Most LDO regulators are trimmed to obtain the most accurate reference voltage possible. However, in some cases the soft-start pin may not be trimmed which results in non-trivial offset voltage remaining in the system during the turn-on period. In those cases, the turn-on period completes slightly faster than expected.

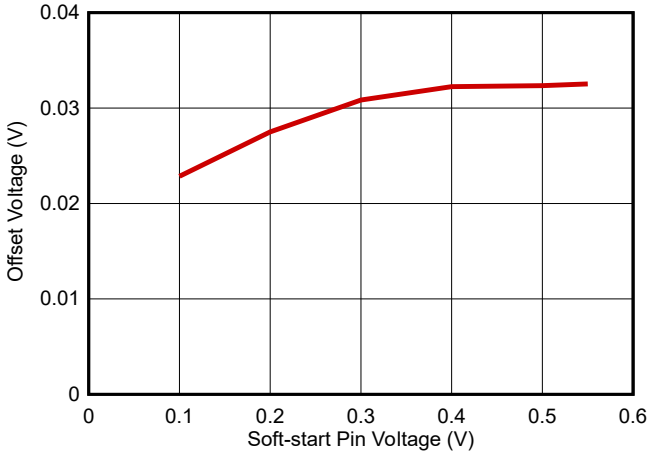
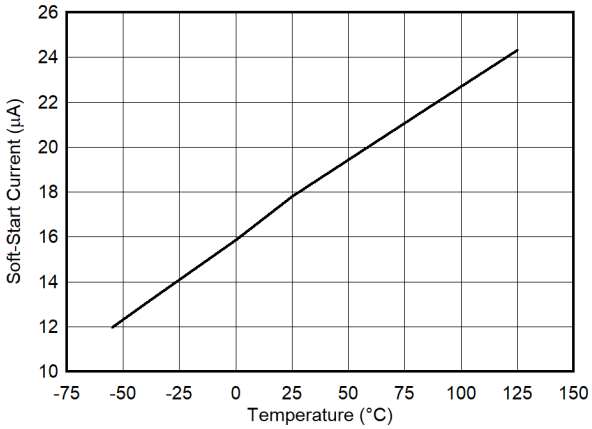



**Figure 2-6. Measured TPS7A74 $V_{OS}$ during turn-on period**

#### 2.1.4.4 Temperature impacts the fast-charge current source

The LDO regulator die temperature momentarily increases during turn on as a result of transient power dissipation while the device charges the output capacitor $C_{OUT}$. This temporary increase in junction temperature can slightly change the proportional to absolute temperature (PTAT) current source used as the soft-start current

source in some devices. Characterization graphs and associated test conditions such as Figure 2-7 are usually included in the device data sheet. During initial turn-on, the higher power dissipation can cause the current source to increase slightly. Near the end of the turn-on period, the power dissipation decreases, which can cause the current source to decrease. Figure 2-8 shows this behavior as a slight curvature in the start-up waveform.




$C_{IN}$ = $C_{OUT}$ = 10µF $C_{BIAS}$ = 1µF $C_{SS}$ = 0nF
$V_{BIAS}$ = $V_{IN}$ = 6V $V_{OUT}$ = 0.65V $V_{EN}$ = 1.5V
$I_{OUT}$ = 0A from the TPS7A74 data sheet

**Figure 2-7. Soft-Start Current vs Temperature**

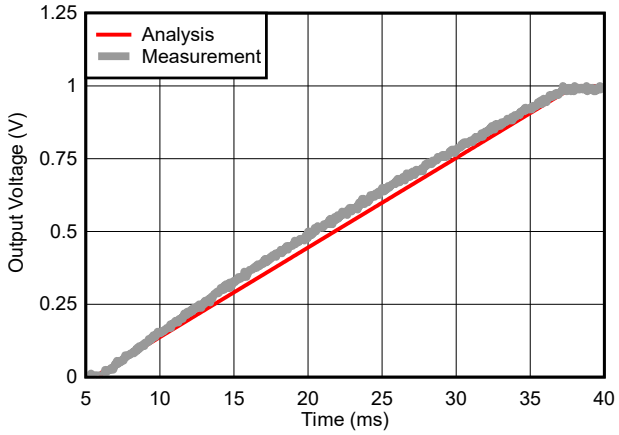



**Figure 2-8. TPS7A74 DC output voltage vs time**

#### 2.1.4.5 Error amplifier common mode voltage

The non-ideal common mode voltage ($V_{CM}$) of the internal error amplifier may induce a sudden step in the LDO regulator turn-on response in older devices. This response is not as pronounced in most modern LDO regulators. LDO regulators that include this induced step response offer a shorter ramp time and longer delay time. The ramp rate of the small voltage step during the initial turn on is a function of the LDO bandwidth, which is different for each LDO regulator. To obtain this ramp rate, it is best to capture a measurement from an EVM after applying the system load. This measurement provides a more accurate evaluation of the device bandwidth.

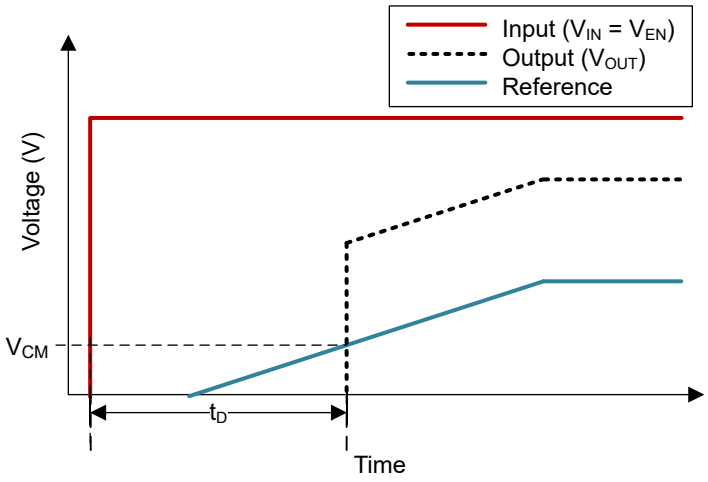



**Figure 2-9. $V_{CM}$ can affect the turn-on time**

#### 2.1.4.6 Reference voltage ($V_{REF}$) ramp time dominates the turn-on time

The reference voltage of most modern LDO regulators turns on much faster than the NR/SS and FF time constants. However, in tracker LDO regulators [3] (where the reference voltage is external to the LDO regulator) this may not be the case. Figure 2-11 and Figure 2-10 show an externally applied reference voltage and the corresponding output voltage of the device.

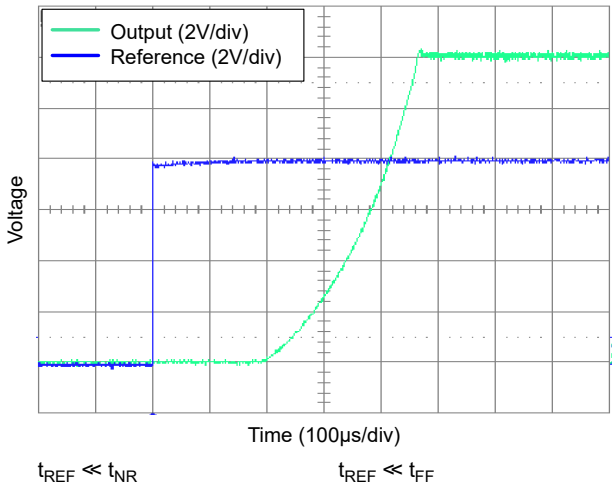



**Figure 2-10. Fast Turn-on Time vs Voltage**

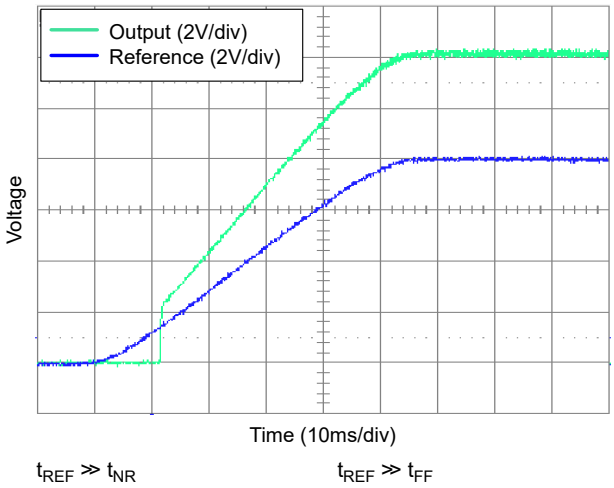



**Figure 2-11. Slow Turn-on Time vs Voltage**

#### 2.1.4.7 Start-up during dropout mode

When a VIN pin and a VEN pin are tied together, and the VIN pin voltage increases slowly, the LDO operates in dropout mode and the output increases at the same rate that the VIN pin voltage increases. There may be overshoot in the output voltage waveform as a result of turning on while operating in dropout mode. [4]

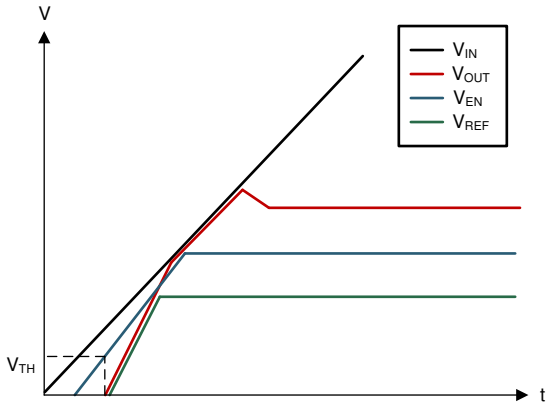



**Figure 2-12. Startup with overshoot**

#### 2.1.4.8 Large values of $C_{OUT}$ induce internal current limit

The turn-on time of an LDO regulator with a significant capacitive load may induce the device to limit the current. In general, the current limit protection of an LDO regulator engages after 20µs to 50µs of operation where the load exceeds the current limit threshold. Thus, the previous discussion applies until current limit is engaged. After current limit engages the LDO approximates a current source charging the output capacitor $C_{OUT}$. Figure 2-13 shows the TPS7A20 loaded with small (1.4µF) output capacitance. While the device remains stable during a range between 0.47µF and 200µF load capacitance, operation at higher values of load capacitance may trigger current limit during startup, slowing down the turn-on time. (See Figure 2-14)

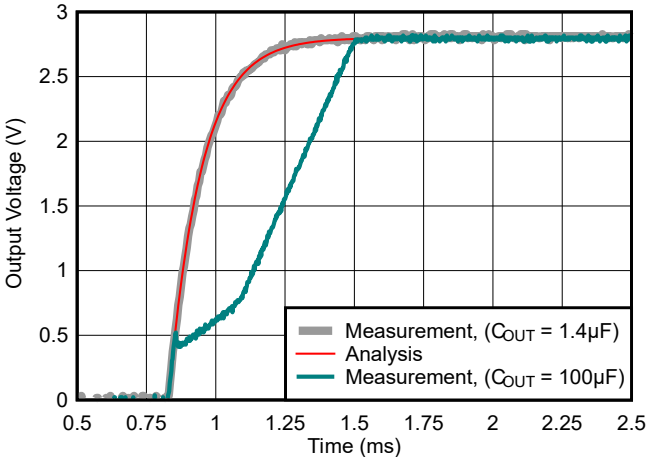



**Figure 2-13. TPS7A20 turn-on comparison**

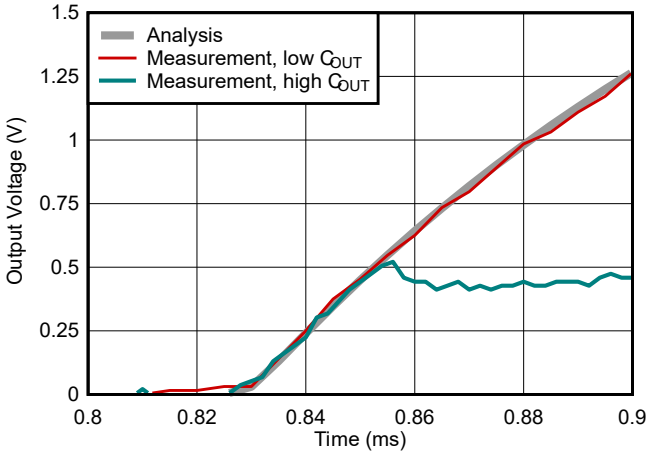



**Figure 2-14. The TPS7A20 current limit engages at approximately 25µs during turn-on**

#### 2.1.4.9 Limitations of large-signal LDO bandwidth

In some LDO regulators, the internal error amplifier bandwidth dominates the turn-on time. Turn-on time is inherently large signal behavior, and the error amplifiers in some devices take longer to respond to such behavior. This response time is especially true of very old devices (such as the LM317 or TLV1117) or of some devices where an amplifier exists between the reference voltage and the NR/SS filter (TPS7A47 for example). It is best to consult the device data sheet for expected turn-on times where the internal bandwidth limits the LDO regulator.

## 2.2 Specific Use Cases and Examples

### *2.2.1 Case 3: Precision voltage reference with $R_{NR/SS}$ and parallel $I_{FC}$ fast charge*

If Figure 2-1 describes the LDO architecture, and the fast-charge circuit uses $I_{FC}$, Equation 6 can be rewritten as Equation 16 after $t > t_{CO}$. Use Equation 11 through Equation 15 and Equation 16 to calculate the turn-on time for these LDO regulators.

When $t \le t_{CO}$, use Equation 13 to calculate $V_{FB}(t)$.

When $t > t_{CO}$, use Equation 16 to calculate $V_{FB}(t)$.

$$V_{FB}(t) = \left(V_{REF}(t) + I_{FC} \times R_{NR/SS}\right) \times \left(1 - e^{-\frac{t}{\tau_{NR/SS}}}\right) \quad (16)$$

The TPS7A91 uses a precision voltage reference, low pass NR filter, optional external $C_{FF}$ capacitor across $R_{TOP}$, and includes a constant current fast charge circuit. The fast charge current is user selectable using the SS_CTRL pin. $V_{CO}$ is 97% of $V_{REF}$. The EVM was used for the measurements.

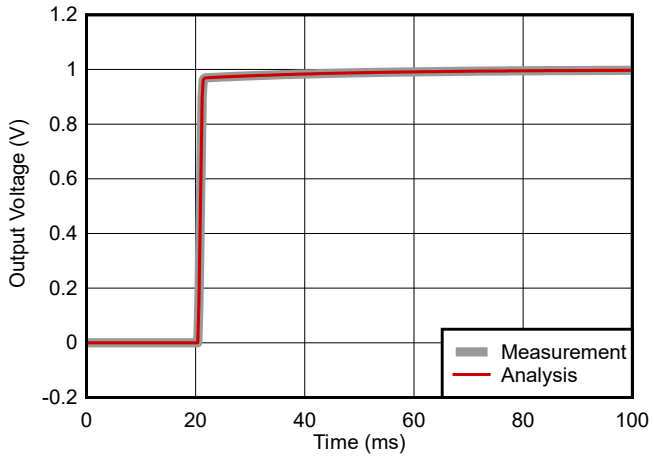



**Figure 2-15. TPS7A49 turn-on time**

### *2.2.2 Case 4: Precision voltage reference with $I_{FC}$ fast charge and no $R_{NR/SS}$*

If Figure 2-1 describes the LDO architecture and the fast charge circuit uses only $I_{FC}$ (that is, $R_{NR/SS}$ disconnects temporarily) then Equation 5 can be rewritten as Equation 17 when $t < t_{CO}$. Equation 11 through Equation 15 and Equation 17 through Equation 20 are used to calculate the turn-on time for these LDO regulators.

When $t \le t_{CO}$, use Equation 17 and Equation 18 to calculate $V_{FB}(t)$ and $V_{TOP}(t)$.

When $t > t_{CO}$, use Equation 13, Equation 15, Equation 19 and Equation 20 to calculate $V_{FB}(t)$ and $V_{TOP}(t)$.

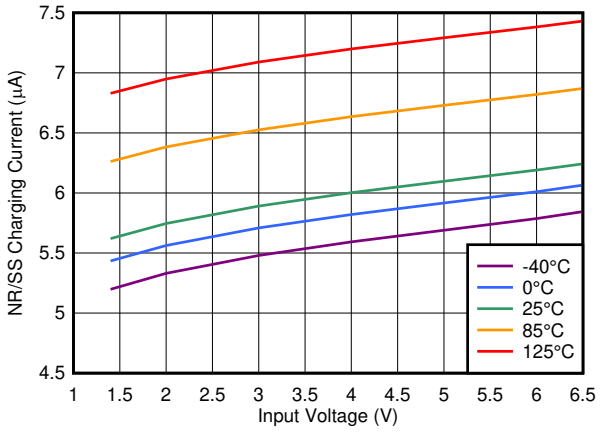
$$V_{FB}(t) = \frac{I_{FC}}{C_{NR/SS}} \times t \tag{17}$$

$$V_{TOP}(t) = V_{FB}(t) \times \left(1 - e^{-\frac{t}{\tau_{FF}}}\right) \tag{18}$$

$$t_{CO} = C_{NR/SS} \times \frac{V_{CO}}{I_{FC}} \tag{19}$$

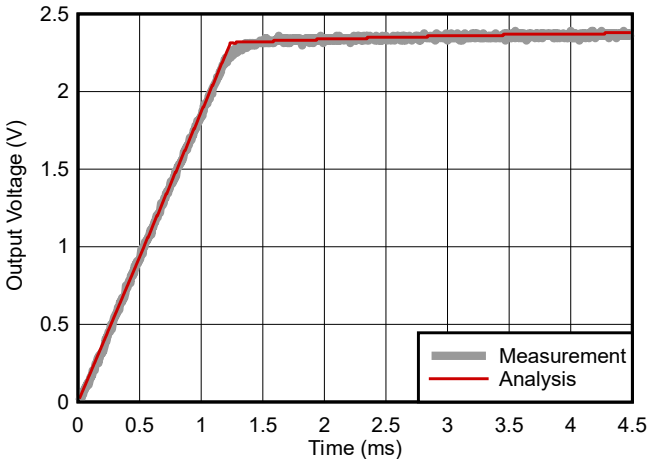
$$V_{CO\_FF} = V_{CO} \times \frac{R_{TOP}}{R_{BOTTOM}} \times \left(1 - e^{-t_{CO}/\tau_{FF}}\right) \tag{20}$$

The TPS7A84A uses a precision voltage reference, low pass NR filter, external $C_{FF}$ capacitor across $R_{TOP}$, and includes a constant current fast charge circuit. Figure 2-16 from the TPS7A84A data sheet describes the fast charge current versus input voltage and temperature. $V_{CO}$ is 97% of $V_{REF}$. The $C_{NR/SS}$ capacitor is rated for 50V and the effective capacitance is nearly constant at 9.6nF. The EVM was used for the measurements.




from TPS7A84A data sheet $V_{BIAS}$ = 0V

**Figure 2-16. Fast-charge current vs input voltage**




TPS7A84A EVM $V_{OUT}$ = 2.4V

**Figure 2-17. DC output voltage vs time**

### *2.2.3 Case 5: Precision current reference*

If Figure 2-2 describes the LDO architecture, $V_{REF}$ can be written as Equation 21 or Equation 22. Use Equation 5 and Equation 7 with Equation 21 for calculations during the fast charge time. Use Equation 13, Equation 15, Equation 22 and Equation 23 for calculations after the changeover event occurs.

When $t \le t_{CO}$ use Equation 21 to calculate $V_{REF}$.

$$V_{REF} = I_{FC}(t) \times R_{NR/SS} \tag{21}$$

When $t > t_{CO}$ use Equation 22 to calculate $V_{REF}$.

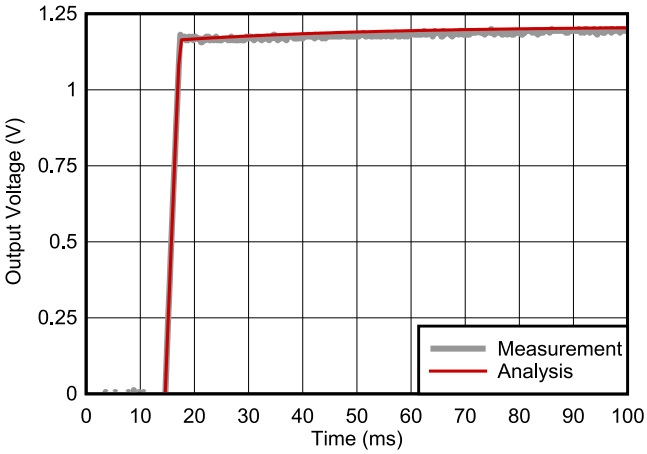
$$V_{REF} = I_{NR/SS}(t) \times R_{NR/SS} \tag{22}$$

$$t_{CO} = -\tau_{NR/SS} \times \ln\left(1 - \frac{V_{CO}}{I_{FC} \times R_{NR/SS}}\right) \tag{23}$$

Figure 2-18 shows the rise time for the TPS7A96 (and the lower current version, the TPS7A94) which uses a precision current reference with an NR/SS pin. During startup the LDO uses a fast charge circuit to rapidly turn on $V_{OUT}$. The TPS7A94 and TPS7A96 have a unique feature in that $V_{CO}$ is programmable using the FB_PG pin and external resistor dividers. In this test using an EVM, $V_{CO}$ is programmed using the external FB_PG resistors and is set to 97% × $V_{OUT}$ = 1.164 V. These LDO regulators operate in unity gain feedback, thus $V_{TOP}$ = 0V.

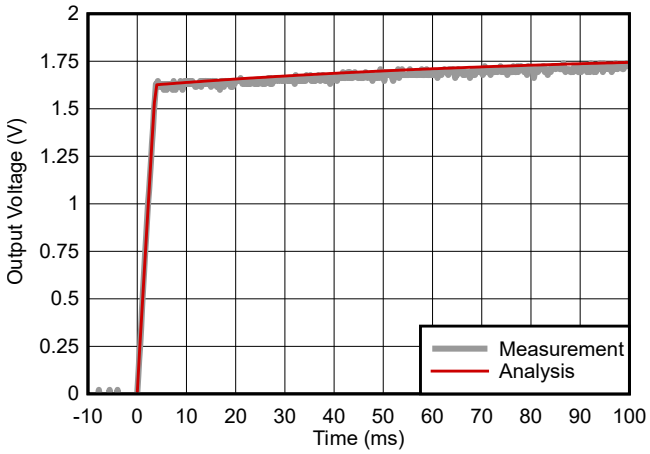
Figure 2-19 shows the rise time for TPS7H1111 which is similar to the TPS7A94 and TPS7A96, except the TPS7H1111 is optimized for power devices in a space environment. In this test using an EVM, $V_{CO}$ is programmed using the external FB_PG resistors and is set to $V_{OUT}$ = 1.626 V. These LDO regulators operate in unity gain feedback, thus $V_{TOP}$ = 0V.

Figure 2-20 shows the test using a TPS7A57 EVM. $V_{CO}$ is internally set to 97% × $V_{OUT}$ = 1.164 V. These LDO regulators operate in unity gain feedback, thus $V_{TOP}$ = 0V.



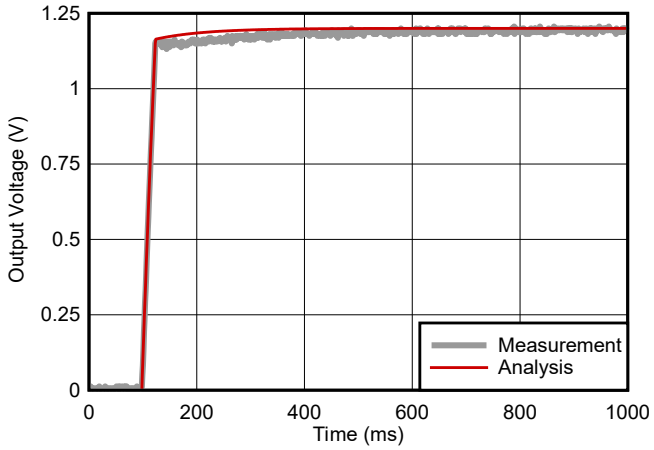

$R_{NR/SS}$ = 8.06kΩ
$I_{FC}$ = 2.1mA
$C_{NR/SS}$ = 4.7µF
$V_{OUT}$ = 1.2V
$I_{NR/SS}$ = 150µA
TPS7A96 EVM

**Figure 2-18. TPS7A96 rise time**




$R_{NR/SS}$ = 18kΩ
$I_{NR/SS}$ = 100µA
$C_{NR/SS}$ = 4.7 µF
$I_{FC}$ = 2.1mA
$V_{OUT}$ = 1.8V
TPS7H1111 EVM

**Figure 2-19. TPS7H1111 rise time**




$R_{NR/SS}$ = 24kΩ
$I_{NR/SS}$ = 50µA
$C_{NR/SS}$ = 3.8µF
$I_{FC}$ = 200µA
$V_{OUT}$ = 1.2V
TPS7A57

**Figure 2-20. TPS7A57 rise time**

### *2.2.4 Case 6: Soft-start timing*

Some LDO regulators use a soft-start (SS) pin that is different than the combination noise reduction and soft-start (NR/SS) pin already discussed. Devices that include a SS pin include the TPS7A74, TPS74401, and TPS748A. While the SS pin programs the $V_{OUT}$ rise time, unlike the NR/SS pin it does not reduce the device noise. Using a soft-start pin, and assuming no $C_{FF}$ is installed, the output rises linearly by tracking the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The same analysis and equations are used as shown in Section 2.1.3, except $V_{CO} = V_{REF}$ in these LDO regulators.

Modern LDO regulators are trimmed to provide excellent accuracy during steady state. However, any device that includes a soft-start pin may not be trimmed during turn-on and a non-negligible $V_{OS}$ may affect the turn-on behavior. This behavior includes slightly faster turn on-time (positive $V_{OS}$) than originally anticipated, as well as a small voltage step in the output voltage during initial turn on.

After $t > t_{CO}$, $V_{CO\_FF}$ is calculated using Equation 25 while setting $t = t_{CO}$ and $V_{FB}(t) = V_{REF}$.

When $t \leq t_{CO}$, use Equation 24 and Equation 25.

When $t > t_{CO}$, use Equation 15 and Equation 19.

$$V_{FB} = \left(\frac{I_{FC}}{C_{SS}} \times t\right) + V_{OS} \quad (24)$$

$$V_{TOP}(t) = V_{FB}(t) \times \left(\frac{R_{TOP}}{R_{BOTTOM}}\right) + \left(\frac{I_{FC}}{C_{SS}} \times \frac{R_{TOP}}{R_{BOTTOM}} \times \tau_{FF}\right) \times \left(e^{-t/\tau_{FF}} - 1\right) \quad (25)$$

The TPS7A74 uses a precision voltage reference with a SS pin. The soft-start current variation with temperature is described in Figure 6-37 in the TPS7A74 data sheet [6]. The offset voltage during turn-on is shown in Figure 2-6. $V_{CO} = V_{REF}$ and Equation 7, Equation 11 through Equation 14, Equation 17 through Equation 20 are used for the analysis. The EVM was used for the measurements with a derated value of $C_{SS}$ = 825 nF according to the capacitor manufacturer. The comparison between the analysis and measurement is provided in Figure 2-8 .

# 3 System Considerations

## 3.1 Inrush current calculation

Use the previous sections to determine the turn-on time for your LDO regulator. Use Equation 26 to calculate the inrush current using the loading on the output of the LDO regulator. The inrush current is a function of output current, output voltage rise time and output capacitance. While quiescent current of the LDO regulator does add to the inrush current, in practice this is a very small fraction of the total inrush and can usually be neglected in the analysis.

$$I_{INRUSH} = I_Q + I_{LOAD} + C_{OUT} \times V_{OUT}(t) \cong I_{LOAD} + C_{OUT} \times V_{OUT}(t) \quad (26)$$

As inrush current increases the LDO regulator temperature rise can temporarily also increase. In rare cases, the internal bond wires can fuse if the inrush current is very high [16]. Fortunately, neither prove to be a major concern in modern LDO regulators in the vast majority of applications. Turn-on times for most LDO regulators are sufficiently fast such that the junction temperature does not significantly rise and place the device into thermal shutdown mode. The current limit protection circuit engages within 20µs to 50µs in most cases, preventing an abnormally high inrush current from fusing the internal bond wires. If heavy inrush exists before the current protection circuit can engage, the fusing current can be reviewed by sending an E2E request to TI. Thus, most concerns regarding inrush current are systematic in nature, such as possible brownout of input supplies, or voltage droop of the input capacitance, $C_{IN}$, due to excessive inrush current.

Figure 3-1 shows inrush current measured in three locations (A, B, and C). D describes an optional damping network.

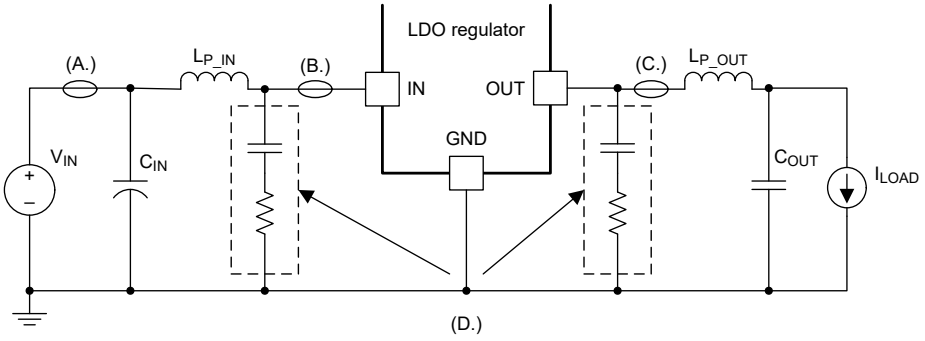



**Figure 3-1. Inrush current probe measurement locations**

Location A is a common measurement point but this may not accurately reflect the true inrush seen through the LDO regulator. The input capacitor, $C_{IN}$ provides some of the current to the device, so measurement point A shows less peaking in the current measurement and a lengthened current pulse.

Location B is the preferred measurement point if the objective is to capture the entire inrush current through the LDO regulator. Inductance ($L_{P\_IN}$) associated with the current probe measurement typically results in excessive ringing in the measurement. An optional damping network can be installed to remove most of this ringing and clean up the measurement significantly.

Location C is the least preferred inrush measurement point. Inductance ($L_{P\_OUT}$) associated with the current loop results in excessive ringing during the turn-on measurement, affecting both the output voltage and the input voltage measurements. Adding a damping network can improve the measurement, however the inductance may continue to slow the turn on time of the VOUT pin. Thus, even when an installed damping network exists, the measurement may not reflect true device performance when the current probe loop is removed.

## 3.2 Inrush current analysis

We can use the previous equations to quickly calculate the inrush current through the LDO regulator if we know the output capacitance and load during the turn-on period. Figure 3-3 provides an example using the TPS7A20 (recall that this device includes an NR filter that also controls the turn-on time). Two 1µF capacitors are installed on the output which provide an effective capacitance of 1.4µF.

Figure 3-3 provides an example using the TPS7A84A. Recall that the TPS7A84A uses a fast-charge current source (without an NR resistor in parallel) and switches in the NR filter for steady state operation. The analysis used $C_{OUT}$ = 67µF and the peak current ($I_{PEAK}$) is well within the tolerance of the capacitors.

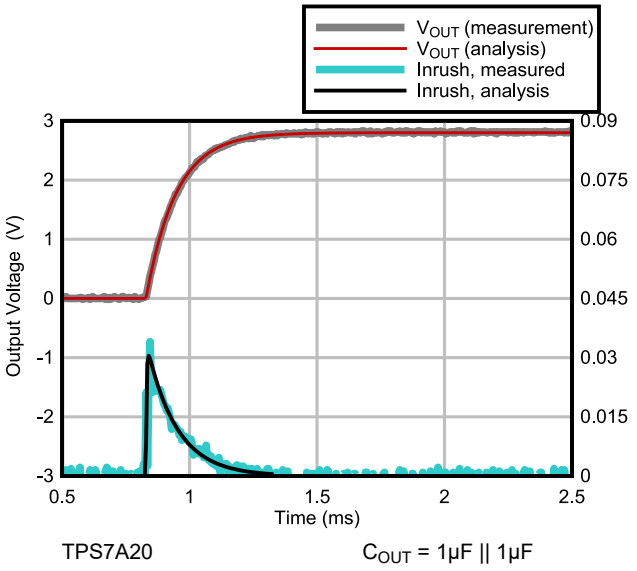



**Figure 3-2. TPS7A20 turn-on with inrush current analysis**

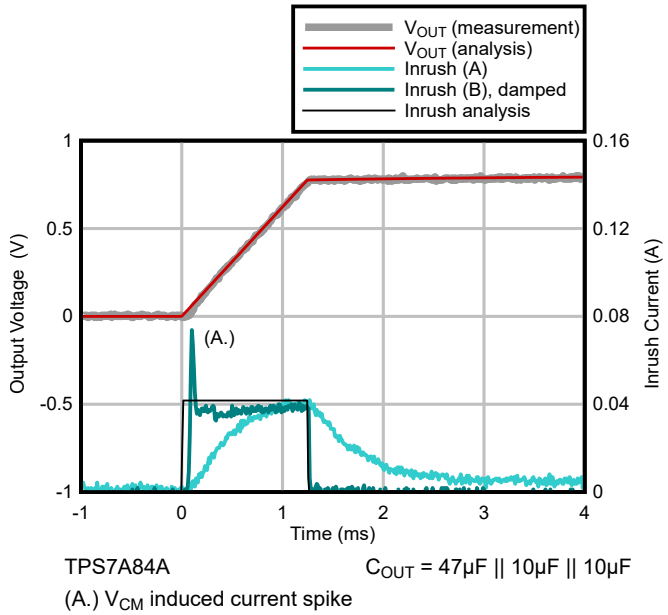



**Figure 3-3. TPS7A84A turn-on with inrush current analysis**

## 3.3 Maximum slew rate

In some applications the LDO regulator must limit the slew rate during the turn-on period [17] , [18], and [19], and the most desirable way to achieve this requirement is to adjust the $C_{NR/SS}$ or $C_{FF}$ capacitance. These slew rate requirements may be enforced across a narrow range of turn on, such as between 2V and 4V of a 5V output, or across the entire voltage range from 0V to steady state. In general, it may be more challenging to meet these requirements using a device with an exponentially rising output as shown in Figure 3-4 than a linear ramp as shown in Figure 3-3. To slow down a fixed output LDO regulator where the NR filter and feedback resistors are internal to the device, the only option remaining is to increase the output capacitance, $C_{OUT}$ such that the current limit loop engages approximately 20µs to 50µs into the turn-on period.

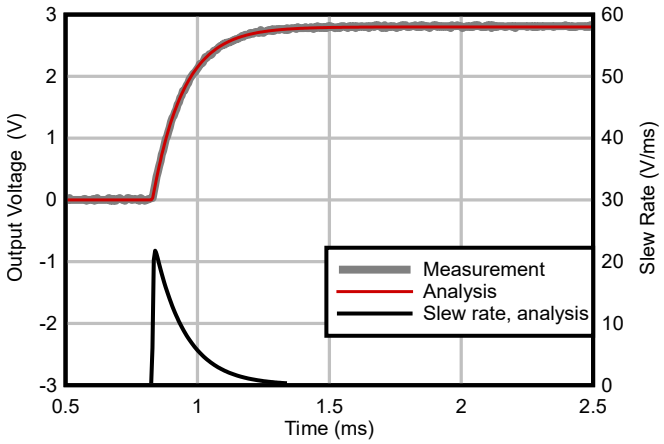



**Figure 3-4. TPS7A20 output voltage slew rate**

## 4 LDO regulators referenced in this paper

| Case | TI LDO Regulators |
|---|---|
| Case 1 | TPS7A20, TPS7A21 |
| Case 2(1) | TPS7A13, TPS7A14, TPS7A49 |
| Case 3 | TPS7A91, TPS7A92 |
| Case 4 | TLV702, TLV703, TLV755P, TPS7A52, TPS7A53, TPS7A53B, TPS7A54, TPS7A83A, TPS7A84A, TPS7A85A |
| Case 5 | TPS7A57, TPS7A94, TPS7A96, TPS7H1111-SP |
| Case 5b | TPS74401, TPS7A74, TPS74701, TPS74801, TPS74901 |

(1) With very small or unpopulated feedforward capacitance ($C_{FF}$), these devices operate using the analysis for Case 1.

## 5 Conclusion

This paper documents the first of its kind framework to define a startup analysis of LDO regulators using either NR filters, feedforward capacitors, or both. The framework includes the impact of fast charge circuitry, and both types of internal precision references of LDO regulators are addressed (voltage references and current references). This paper discusses non-ideal characteristics of modern LDO regulators, and how they impact the LDO startup times. Designers can use this framework to calculate turn-on ramp times and LDO inrush current, and they can assess the output voltage slew rate during turn-on time to confirm that the LDO startup behavior meets their system requirements.

## 6 References

1. Thomas, Roland E., Rosa, Albert J. *The analysis and design of linear systems*, 4th ed. ISBN 978-1118065587
2. Lathi, B.P. *Signal Processing & Linear Systems* ISBN 978-0195219173
3. Texas Instruments, data sheet: *TPS7A20 300-mA, Ultra-Low-Noise, Low-$I_Q$, High PSRR LDO*
4. Texas Instruments, data sheet: *TPS7A49 36-V, 150-mA, Ultralow-Noise, Positive Linear Regulator*
5. Texas Instruments, data sheet: TPS7A91 1-A, High-Accuracy, Low-Noise LDO Voltage Regulator
6. Texas Instruments, data sheet: TPS7A74 1.5-A, Low-Dropout Linear Regulator With Programmable Soft-Start
7. Texas Instruments, data sheet: TPS7B4250-Q1 50-mA 40-V Voltage-Tracking LDO With 5-mV Tracking Tolerance
8. Liu, Jason. "Various Applications for Voltage-Tracking LDO." Texas Instruments application report, literature No. SLVA789, 2016
9. Texas Instruments, application report: Zhang, Penn, and Jason Song. *Avoid Start-Up Overshoot of LDO*.
10. Texas Instruments, data sheet: *TPS7A84A 3-A, High-Accuracy (0.75%), Low-Noise (4.4-$\mu V_{RMS}$) LDO Regulator*
11. Texas Instruments, data sheet: *TPS7A96 2-A, Ultra-Low Noise, Ultra-High PSRR, RF Voltage Regulator*
12. Texas Instruments, data sheet: *TPS7H1111-SP and TPS7H1111-SEP 1.5-A, Ultra-Low Noise, High PSRR Radiation Hardened Low Dropout (LDO) Linear Regulator*
13. Texas Instruments, data sheet: *TPS7A57 5-A, Low-$V_{IN}$ (0.7 V), Low-Noise (2.1 $\mu V_{RMS}$), High-Accuracy (1%), Ultra-Low Dropout (LDO) Voltage Regulator*
14. Texas Instruments, data sheet: *TPS74401 3.0-A, Ultra-LDO with Programmable Soft-Start*
15. Texas Instruments, data sheet: *TPS748A 1.5-A, Low-Dropout Linear Regulator With Programmable Soft-Start*
16. G. T. Nobauer and H. Moser, *Analytical approach to temperature evaluation in bonding wires and calculation of allowable current, in IEEE Transactions on Advanced Packaging*, vol. 23, no. 3, pp. 426-435, Aug. 2000
17. Renesas, application note: *Overcoming Minimum Vdd Ramp Rate Limitation*
18. TI E2E Forum
19. Texas Instruments, data sheet: *AM64x Sitara™ Processors*, Section 6.10.2.1
20. *DC and AC Bias Dependence of Capacitors Including Temperature Dependence*, DesignCon East 2011
21. Stephen Ziel, *Tips, tricks and advanced applications of linear regulators*, Texas Instruments Power Supply Design Seminar SEM2600, 2024

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